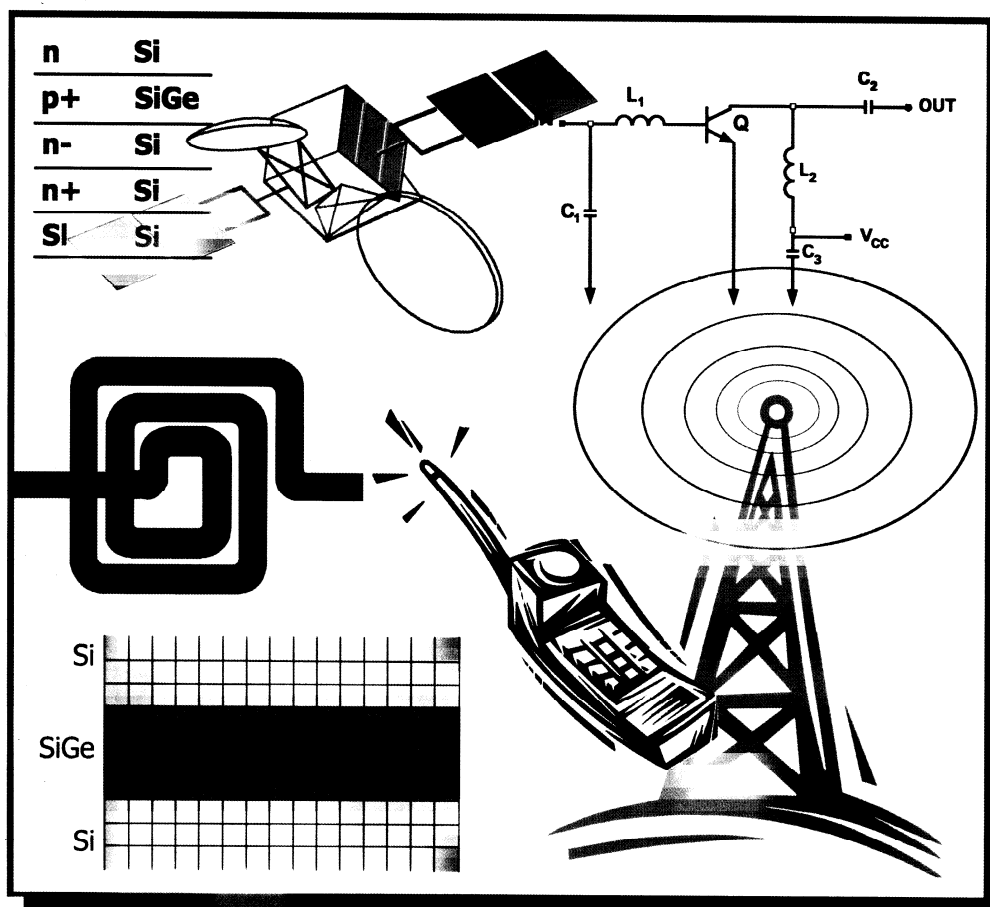


2006

Topical Meeting on Silicon Monolithic Integrated Circuits in RF Systems



18–20 January 2006 • San Diego, California, USA

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**2006 Topical Meeting on
Silicon Monolithic Integrated Circuits
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DIGEST OF PAPERS

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IEEE Catalog Number 06EX1204

ISBN 0-7803-9472-0

Library of Congress 2005932183

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Silicon-Based Nanomembrane Materials: The Ultimate in Strain Engineering

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Abstract — The lattice-mismatch-induced strain in growth of Ge on Si produces a host of exciting scientific and technological consequences, both in 3D nanostructure formation and, when silicon-on-insulator (SOI) is used as a substrate, in 2D membrane fabrication. One can use the ideas of strain sharing and critical thickness, combined with the ability to release the top layers of SOI, to create free-standing, dislocation-free, elastically strain relieved flexible Si/Ge membranes with nanometer scale thickness, which we call NanoFLEXSi or Si nanomembranes (SiNMs). The membranes can be transferred to new substrates, producing the potential for novel heterogeneous integration.

The very interesting, and in some cases surprising, structural and electronic properties of these very thin membranes have been revealed using STM, x-ray diffraction, and electronic transport measurements. For example, STM shows that conduction in very thin Si layers on SOI with bulk-Si mobilities is possible even though the membrane is bulk depleted. Using the effect of elastic strain, we have fabricated two-dimensional electron gases (2DEGs) in membrane structures; we support the transport measurements with calculations suggesting that we are observing a single bound state in the well. We have fabricated thin-film transistors (TFTs) that we have transferred to flexible-polymer hosts that show a very high saturation current and transconductance. Thus very high-speed flexible electronics over large areas become possible.

Index Terms — flexible electronics, Si nanomembrane, elastic strain relief, strained Si, 2DEG, thin-film transistor.

I. INTRODUCTION

Strain engineering on Si-based material has spurred intense research over the past decade. Substantial carrier mobility enhancement on tensile-strained Si surface long-channel MOSFETs has been demonstrated: up to 80 % for electrons and 100 % for holes compared with unstrained bulk Si [1]-[2]. In the sub-100 nm gate length regime, very impressive performance enhancement of both n-type and p-type strained-Si MOSFETs has also been reported [3]-[4], making strained Si a strong candidate for advanced CMOS technology. The biaxial tensile stress splits the six-fold degenerate conduction band in Si into a higher-energy four-fold degenerate valley and a lower-energy two-fold

degenerate valley. At the same time strain modifies the valence band structure by lifting up the light-hole band and lowering the heavy-hole and spin-orbit bands. Thus, electron and hole mobility enhancement is contributed from the reduced intervalley and interband scattering, and also from the reduced effective masses [5]-[6]. Furthermore, because the strain modifies the band structure (in this case the conduction band), a strained thin Si layer sandwiched between two relaxed SiGe layers combined with an additional n-type doping layer is widely used to create a 2-D electron gas (2DEG) structure [7]-[8]. 2DEGs generate much interest in Si-based quantum dots and high-performance devices, such as modulation-doped FETs (MODFETs).

To strain the Si, the most widely used technique is to grow it on a strain-relaxed SiGe virtual substrate, which in turn is created by growing strain-graded SiGe layers on bulk Si [9]-[10]. Strain relaxation occurs, once the SiGe layer thickness exceeds the critical thickness for pseudomorphic growth, by the movement of dislocations through the SiGe layers. Misfit dislocations at the interfaces between the layers (created by the strain differential between the layers) relax the strain. Every misfit dislocation has two threading arms associated with it that extend through the entire film system, including the ultimate strained-Si layer. Hence, whereas the misfit dislocations at the strained Si-SiGe interface can be reduced by strain grading, the threads remain. Scattering of charge carriers by these threads can degrade the carrier mobility [11]. Additionally, the relaxation process in the SiGe layers generates steps at the SiGe surface through the opening of dislocation loops there. These steps bunch, creating a rough growth front referred to as cross-hatch. A polishing and cleaning step is then necessary before further device processing. Thus, one of the main challenges to obtaining high-quality strained Si is in obtaining a perfect strain-relaxed SiGe substrate.

To address this problem, various techniques have been realized, such as efforts to find compliant substrates, which would allow the strained-film system to relax by

sliding freely on the substrate at elevated temperature [12]-[13], and elastic strain-sharing on the free-standing portion of a single-point supported mesa [14]-[15]. Compliant substrates exist only in very special cases. The promised benefits of compliant substrates can, in fact, be achieved with SiNMs. We describe here fabrication of SiNMs and some applications. We demonstrate both remarkable strain and band structure engineering on tens of mm^2 area membranes, and high-performance FETs fabricated on these highly transferable nanomembranes on flexible-host substrates.

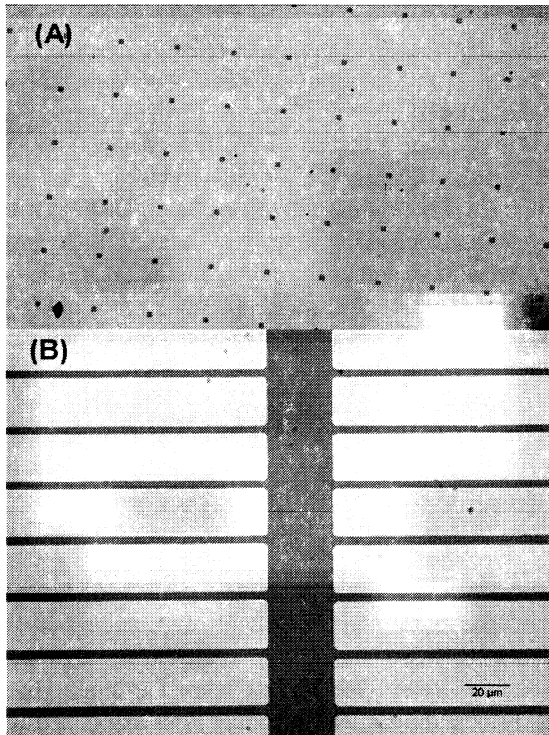


Fig. 1 Optical micrograph of (A) a $1.8 \text{ mm} \times 1 \text{ mm}$ part of a released $4 \text{ mm} \times 4 \text{ mm}$ membrane transferred in solution to an oxidized Si wafer. (B) Si strips with $20 \mu\text{m}$ width separated by $5 \mu\text{m}$ transferred to a flexible substrate by dry printing.

II. FROM 3-D TO 2-D

A. NanoFLEXSi Fabrication

To fabricate NanoFLEXSi, we grow epitaxial layers of bottom Si, SiGe alloy, and top Si layers on a UNIBOND SOI substrate by chemical vapor deposition (CVD) at 580°C in a cold-wall ultra-high-vacuum CVD reactor [16]. High-purity diluted SiH_4 and GeH_4 gases are used for Si and SiGe growth; both n-type and p-type doping are possible by incorporating PH_3 and B_2H_6 gases. The sample was heated by resistance heating and the growth pressure

was 30 mTorr with a base pressure of 10^{-10} Torr. The growth was in-situ monitored with reflection high-energy electron diffraction (RHEED) to determine a 2-dimensional growth (planar growth) or 3-D (i.e., hut and/or dome formation). The thickness of the SiGe alloy is limited by the kinetic critical thickness, which is ~ 100 and $\sim 150 \text{ nm}$ for 20 % and 15 % Ge fraction at 580°C growth temperature [17]. Si layers are generally much thinner than the alloy layer and the total film thickness (including the SOI template) is on the order of 200 nm. The thickness considerations for the Si layers will be described in next subsection.

If unbalanced strain is desired, the final structure on top of the buried oxide (BOX) can consist of only the bottom Si and the SiGe alloy layer. On the other hand, if balanced strain is desired, the layer can be a Si-SiGe-Si sandwich structure with same or similar thicknesses of the top and bottom Si. For the as-grown structure, Si layers retain their lattice constant because of the confinement from the BOX, which results in compressive strain on the SiGe layer only. The higher the Ge fraction is in the alloy layer, the higher the strain in the alloy layer. However, the maximum thickness allowed before the SiGe would relax through dislocation generation also decreases. To create NanoFLEXSi with tensile-strained Si, the as-grown structure is patterned into squares with small mesh holes or narrow strips by conventional optical photolithography followed by RIE to expose the underlying BOX. The photoresist is completely striped before immersing the sample into 49 % HF to undercut the BOX. The immersion time is chosen so the BOX under the as-grown structure can be completely removed. So obviously the larger the pitch of the mesh holes (Fig. 1A) or the wider the strips (Fig. 1B), the longer is the HF immersion time. During the BOX removal, the free-standing part of membranes settles on the Si handling substrate as the etching front propagates and registers itself via a weak van der Waals force to the underlying Si at almost the exact location as just patterned [15]. Completely undercut membranes, when the area is small (tens of μm^2) can detach from the Si handling wafer during the DI water rinse and float off on the surface of the water. For large-area membranes, a solvent such as IPA is introduced in the end of DI water rinse to facilitate the separation between membranes and Si handling wafer. Once they separated the membranes floated in the solvent and demonstrated remarkable flexibility. They can fold and unfold many times without cracking.

When the membranes are fully released they are easy to transfer to new hosts by picking them up using a desired substrate. So far, we have transferred released membranes as large as $5 \text{ mm} \times 5 \text{ mm}$ to glass, H-terminated Si, oxidized Si, Teflon, and metal grids. We have also

developed a simple dry printing technique that transfers the fully undercut membranes by pressing the sample against an adhesive material [18]. This technique has successfully transferred the membranes to flexible polymer hosts with high transfer rate. Fig. 1(A) shows an optical micrograph of part of a 4 mm × 4 mm elastically strain-sharing 45 nm Si / 130 nm Si_{0.84}Ge_{0.16} / 45 nm membrane transferred in solution to an oxidized Si wafer. The transferred membrane shows few visible wrinkles or cracks over the entire 16 mm² area. Fig. 1(B) shows a 200 nm Si membrane patterned into 20 μm wide × 1 mm long strips and were transferred to a flexible polymer (PET) host via a dry printing technique (see below). The gap between the transferred strips remains at the 5 μm that was patterned on the starting SOI substrate, indicating a faithful transfer method.

B. Strain Engineering and Band Structure Modification

As mentioned above, elastic strain sharing occurs upon the removal of the underlying BOX. If we assume an ideal elastic system and coherent interface between Si and SiGe layers, the strain distributed between the SiGe alloy and the top and bottom Si layers can be calculated using

$$\epsilon_{SiGe} = \epsilon_m \frac{h_{Si} M_{Si}}{h_{SiGe} M_{SiGe} + h_{Si} M_{Si}} \quad (1)$$

$$\epsilon_{Si} = -\epsilon_m \frac{h_{SiGe} M_{SiGe}}{h_{SiGe} M_{SiGe} + h_{Si} M_{Si}} \quad (2)$$

where ϵ_m is the mismatch strain, and ϵ , M , and h are the layer strain, biaxial moduli, and thicknesses of Si (include top and bottom) and SiGe layers [19]. Clearly, if large strain is desired in the Si layers, larger mismatch strain (ϵ_m) and/or a larger SiGe to Si thickness ratio are preferred. Because there is a tradeoff between Ge fraction and critical thickness of the alloy layer, a thin Si template layer on the starting SOI substrate is preferred for maximum strain transfer.

To confirm that the release process causes elastic strain sharing in the NanoFLEXSi membrane, we made x-ray diffraction (XRD) reciprocal-space maps of the structure to determine the strain, thickness, and composition of the layer system both before and after its release. Fig. 2(A) shows the map of the as-grown layers. Because the Si layers are not strained before release, their peaks coincide with the Si handling substrate (same 2θ angle), as expected. The peak for the SiGe alloy occurs at a much smaller diffraction angle, because of its larger out-of-plane lattice constant. We determine from the data fitting of a theta / 2-theta line scan that the layer structure from top to bottom is 48 nm Si, 128 nm Si_{0.84}Ge_{0.16}, and 56 nm Si

(include the 20 nm Si template of the SOI). After releasing and transferring a 4 mm × 4 mm area membrane to a new Si (001) substrate, XRD shows both SiGe and Si peaks shift *rigidly* to higher angle (Fig. 2(B)), which means the strain relief from the SiGe alloy has transferred to Si layers to the degree allowed by Eqs. (1) and (2). The Si thin films now have a larger in-plane lattice constant (tensile strained) and smaller out-of-plane lattice constant, so higher 2θ. The shift is 0.091 ± 0.008° which corresponds to a tensile strain in the Si layers in the transferred membrane of 0.3 ± 0.02 % and a compressive strain in the SiGe layer of 0.29 ± 0.02 %. In agreement with Eq. (1) and (2), for the thickness ratio we have in this sample (SiGe / Si = 128 / 104 = 1.23), around 50 % of strain in the SiGe layer has been transferred to the two Si layers.

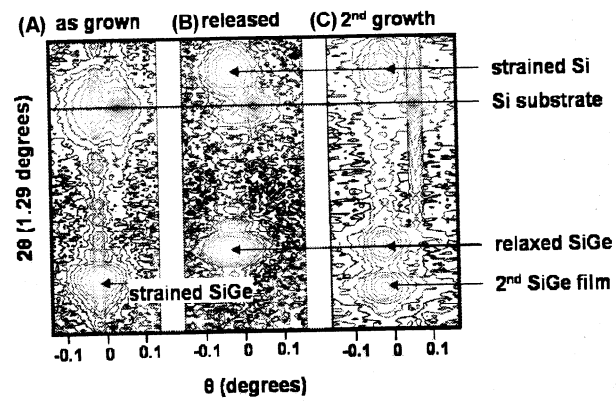


Fig.2 XRD reciprocal-space maps at several Si/SiGe/Si membrane conditions. (A) The Si/SiGe/Si film stacks as grown on a SOI substrate. (B) The released membrane transferred to a new oxidized Si substrate. Both Si thin-film and SiGe alloy peaks shift to a higher 2θ angle due to strain sharing. (C) The transferred membrane after deposition of a second SiGe film with higher Ge fraction.

In addition to the strain sharing, the XRD map shows omega (x-axis) peak widths of less than 0.03°. The widths of these diffraction peaks are an order of magnitude narrower than those typically observed in strained Si grown on a strain-graded SiGe substrate [10]. Line scans through the SiGe and Si films have thickness fringes from the finite film thicknesses before and after release. The continued presence after release of the thickness fringes and narrow peak widths are in agreement with dislocation-free relaxation.

The amount of strain that can be achieved in the NanoFLEXSi membrane, as explained above, is dictated by the Ge fraction in the alloy, the critical thickness of the SiGe layer, and the thickness ratio between SiGe and Si

layers. To get even higher strain, one possibility is to grow a higher-Ge-fraction SiGe alloy on the transferred membrane and re-release it. Because the in-plane lattice constant of the Si layer of the released membrane has been enlarged in the first strain sharing process, the lattice mismatch with the now deposited second, higher-Ge-alloy layer is reduced, and it is possible to achieve an even high strain without dislocation formation. Fig. 2(C) shows the XRD map after the growth of a second SiGe film on the released-and-transferred membrane. The diffraction peak of the second SiGe occurs at lower 2θ angle while the Si, and the first SiGe peaks stay at the same position. When this membrane is released for a second time, strain sharing again occurs and the tensile strain in the Si layers increases.

To verify that the strain induces a band structure modification, we grew a modulation-doped heterostructure on a SiGe-on-insulator (SGOI) substrate. The SGOI has a relaxed, 42 nm thick $\text{Si}_{0.8}\text{Ge}_{0.2}$ layer, phosphorus doped at $2 \times 10^{17} \text{ cm}^{-3}$, directly on the BOX. The final structure we grow, from bottom to top consists of 42 nm $\text{Si}_{0.8}\text{Ge}_{0.2}$, 90 nm undoped $\text{Si}_{0.67}\text{Ge}_{0.32}$, a 16 nm undoped Si quantum well, 10 nm undoped $\text{Si}_{0.67}\text{Ge}_{0.32}$, 30 nm $\text{Si}_{0.67}\text{Ge}_{0.32}$ with phosphorus doping at $4 \times 10^{17} \text{ cm}^{-3}$, 20 nm undoped $\text{Si}_{0.67}\text{Ge}_{0.32}$, and a final 8 nm Si cap layer. A Hall bar structure was patterned and etched to a depth of 90 nm, and Au/Sb alloy was evaporated to form ohmic contacts. Before the membrane is released, the Si quantum well was tensile strained at 0.68 %, as determined by XRD. After we completely remove the BOX, the strain increased to 0.93 % as expected. Fig. 3(A) shows the Hall-bar structure patterned on a membrane that settled onto the original Si handling substrate after BOX removal. The in-place settling (i.e., without floating off and transfer to a new substrate) results in some buckling of the film as it elastically expands. We have calculated that while the buckling could cause local strain, the globally strain induced by this buckling is negligible [20]. Four-probe longitudinal magnetoresistance measurements were performed at a temperature of 2 K before and after the release. As shown in Fig. 3(B), the before-release longitudinal resistance shows a pronounced upward curvature typical of a quantum well with more than one occupied subband [21]. The longitudinal resistance after release, on the other hand, shows a flat magnetic-field dependence for small magnetic fields and progressively larger Shubnikov-de Haas oscillation at higher field, which is a hallmark of 2DEG transport in a single subband [22]. We have calculated that following release, the elastic strain relaxation in the thick $\text{Si}_{0.67}\text{Ge}_{0.32}$ layers causes an increase of the tensile strain of the Si quantum well, resulting in an increase in the depth of the quantum well of

approximately 50 meV. The larger band offset enlarges the separation between subbands and results in the occupation of only one subband in the released structure.

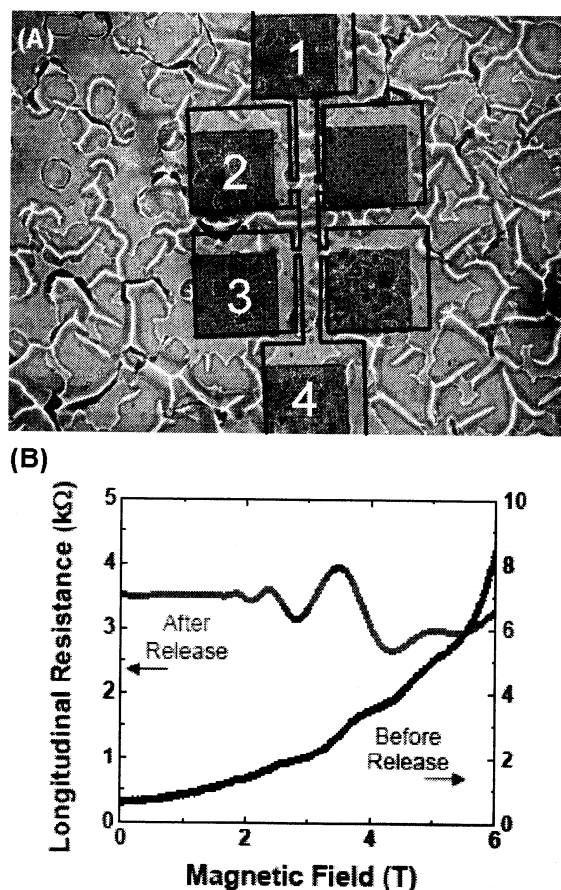


Fig. 3 (A) Image of the released membrane and Hall-bar with ohmic contacts; Hall-bar is outlined for visibility. (B) Longitudinal magnetoresistance before and after release measured at 2 K. Current is from contact 1 to 4; voltage is between 2 and 3.

C. Electrical Properties of MOSFETs Fabricated on NanoFLEXSi

We take advantages of the transferability and also the elastic strain sharing of the NanoFLEXSi membranes and fabricate MOSFETs after transferring the membranes to both solid and flexible hosts. High-temperature fabrication may be employed on device fabrication for membranes transferred to solid hosts such as oxidized Si, while, for most flexible hosts, a low-temperature process must be developed.

NanoFLEXSi has great potential as the device material for high-performance thin-film transistors (TFTs) for future flexible-electronics applications. It provides the advantage of exploiting high-quality, single-crystal Si with

or without elastic strain on flexible substrates, where high performance, such as high carrier mobility and high current drive capability, have always been challenges [23]-[25]. We fabricate n-type TFTs on NanoFLEXSi membranes using a dry-printing technique that transfers the membranes to a flexible host in one simple step [18]. Fig. 4 shows 20 μm wide Si/Si_{0.83}Ge_{0.17}/Si (45/150/50 nm) membrane strips on a ITO coated poly(ethylene terephthalate) (PET) host. SU8-2002 was spun on the PET as adhesive material and the released membrane (settled on Si handling substrate) was brought face down in contact with it. The binding force between SU8-2002 and the membrane is larger than the van der Waals force between the membrane and the Si handling substrate: as a consequence the released membrane is transferred to the new host. The ITO serves as gate electrode and the SU8-2002 as gate dielectric layer. Ti in rectangular shape was formed by evaporation and liftoff on the transferred membrane as source and drain electrodes. The different gaps between the metal pads shown in Fig. 4 correspond to different channel lengths. The temperature is controlled at lower than 120°C throughout the entire process. A representative I-V curve of a 3 μm -channel-length and 60- μm -channel-width TFT is shown in Fig. 5. N-type MOSFET behavior is clearly demonstrated on the transferred sandwich membrane with threshold voltage at around 2.5 V.

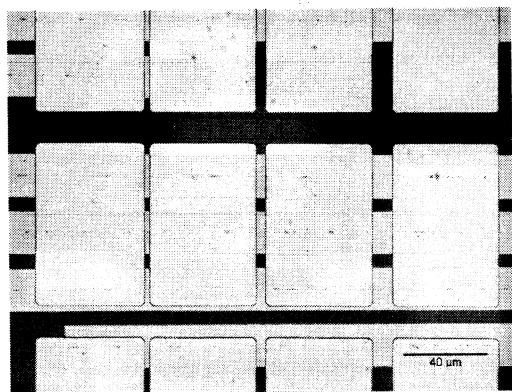


Fig. 4 Optical micrograph of Si/SiGe/Si strips transferred on a flexible host. The width of the strips (orange separated by black gaps) and running horizontally) is 20 μm and the rectangles (bright yellow) are Ti metal serving as source and drain electrodes. Different gaps between these metal pads allow for different channel lengths.

We have conducted XRD measurement and confirmed that elastic strain sharing is not affected by the dry printing technique. The thin Si layers were tensile strained by the partially relaxed SiGe, the same as for the membranes transferred in solution depicted previously. When comparing the DC characteristics with identical TFTs fabricated on a release-and-transferred 200 nm

thick, single-crystal unstrained Si thin film, we find that both the drain current and the transconductance of the TFTs on elastically strained Si membranes are much larger than those on an equivalent unstrained Si membrane

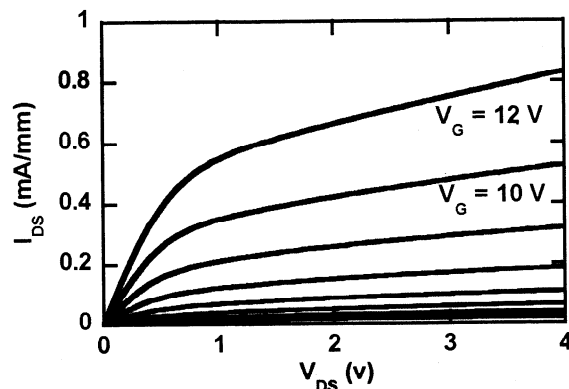


Fig. 5 A representative I-V curve of a Si/SiGe/Si NanoFLEXSi TFT transferred onto a flexible host. The gate length and width are 3 μm and 60 μm , respectively. The gate voltage varies from 12 V to -4 V in a 2 V intervals.

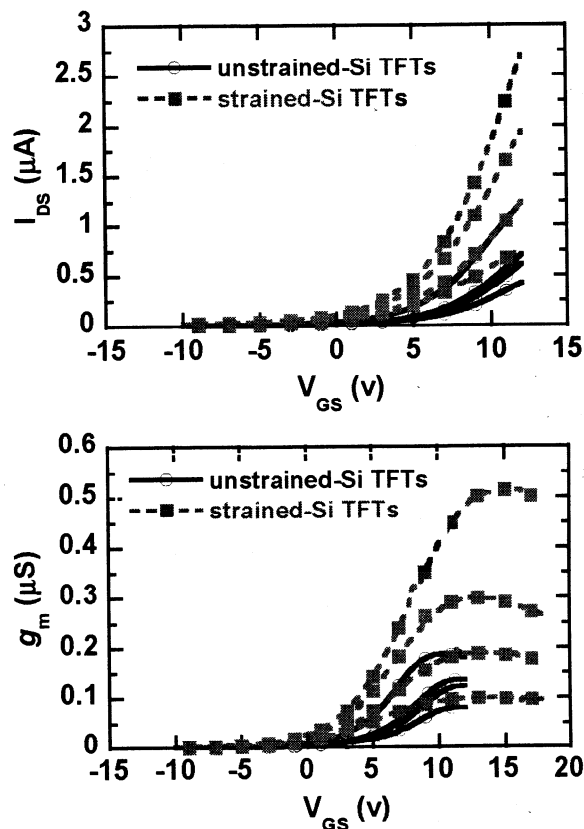


Fig. 6 Comparisons of drain current and transconductance between unstrained-Si and strained-Si (Si/SiGe/Si) TFTs transferred on flexible hosts. The drain-to-source voltage is 50 mV and the gate length from top curve to bottom is 3, 10, 20, and 50 μm .

(Fig. 6). These enhancements, we believe, are caused primarily from the presence of the smaller bandgap SiGe layer. We believe these simple tests demonstrate the promise of NanoFLEXSi for flexible electronics: by using the Si/SiGe/Si material system we can in a straightforward manner produce devices that outperform even the high-performance single-crystal Si.

D. Thin and Thinner

We have described the fabrication and electrical properties of the elastically strain-shared Si/SiGe/Si NanoFLEXSi membrane. So far, the thickness of the membrane is on the order of a few hundreds of nanometers. Ultra-thin-body SOI MOSFETs that consist of less than tens of nanometers thick Si on BOX are considered promising structures for ultimate device scaling [26]-[27]. However, when the Si layer becomes thin enough, charge traps at the oxide-Si interface will deplete the Si layer of free carrier. One would therefore predict that measurement, such as scanning tunneling microscopy (STM) becomes impossible since it depends on the flow of current. Despite of the high resistivity of ultra-thin Si template layers on SOI, we have shown atomic resolution of a 10 nm thin Si template layer (Fig. 7) [28]. So in addition to "bulk", dopant-mediated conduction, there must be another conduction mechanism that makes the STM imaging possible. It has been known that surface states, through the dimer reconstruction on the clean Si (001) surface, consist of bonding (π) and antibonding (π^*) bands with a gap of about 0.5 eV [29]. The Si valence band is close to the middle of the surface states gap. We propose that a large concentration of electrons are thermally excited to the π^* band leading a large concentration of holes in the Si template layer valence band, which effectively pulls the Si Fermi level downward and pins it around the valence band. The effective resistance is now greatly reduced by the holes in the Si layer and the electrons in the surface π^* states, while the carriers at the Si/BOX interface are effectively immobile and do not contribute to the conduction. It is thus the interaction between surface and bulk that enables high-mobility conduction in nano-scale SOI. And through this analysis we conclude that conduction will be possible in very thin layers or membranes of other materials when the surface Fermi level is pinned far from mid-bandgap by surface or interface states.

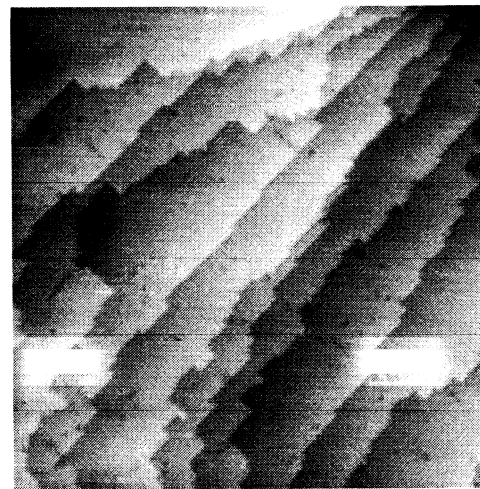


Fig. 7 Filled-state STM image of the surface of a 10 nm thick Si template layer of bonded SOI (001). $V_{\text{sample}} = -2$ V, 100 nm \times 100 nm view.

III. CONCLUSION

We have described here the fabrication and application of NanoFLEXSi membranes. The flexible nature of these Si-based nanomembranes enables us to transfer the membranes literally to any substrate that is not rapidly soluble in water or can be printed on through the usage of appropriate adhesive materials. It provides tremendous possibilities for heterostructure integration. This technique involves minimum dislocation formation, which could potentially be the ultimate in the prospective strained-Si engineering.

ACKNOWLEDGEMENT

This work was supported by DOE, AFOSR, and NSF-MRSEC

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