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Electrical conductivity in silicon nanomembranes

Pengpeng Zhang[1], E P Nordberg[1], B-N Park[1], G K Celler[2], I Knezevic[1], P G Evans[1], M A Eriksson[1] and M G Lagally[1,3]

[1] University of Wisconsin-Madison, Madison, WI 53706, USA
[2] Soitec USA, 2 Centennial Drive, Peabody, MA 01960, USA
E-mail: lagally@engr.wisc.edu

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Abstract. Silicon nanomembranes (SiNMs) are very thin, large, free-standing or free-floating two-dimensional (2D) single crystals that can variously be flat, rolled into tubes, or made into any number of odd shapes, cut into millions of identical wires, used as conformal sheets, or chopped into tiny pieces. Because SiNMs are mostly surface or interface and little bulk, they have very interesting properties. We describe electrical conductivity in SiNMs. Because of trap states at the Si/SiO_2 interface, bulk dopants become irrelevant to electronic transport when the membrane is thin enough. Replacing the oxide at one interface with the clean-Si surface reconstruction dramatically increases the nanomembrane conductivity. We provide a model for this behaviour. The dimer reconstruction surface states provide a means of 'surface doping'. Other materials with proper highest-occupied molecular orbital (HOMO) or lowest-unoccupied molecular orbital (LUMO) bands, when deposited on the Si surface, should produce the same conductivity effect, affording a broad opportunity for membrane-based sensors.

Contents

[3] Author to whom any correspondence should be addressed.

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1. Introduction

Silicon-on-insulator (SOI), in which a Si dioxide layer is interspersed between a crystalline top Si layer (the template or device layer) and the bottom Si (handle) wafer, is becoming the mainstream substrate for microelectronics, offering improved speed and reduced power consumption in comparison to conventional bulk Si [1]–[3]. Beyond that, SOI serves as the foundation of a nascent nanotechnology, based on the ability to etch the buried oxide selectively to free very thin Si membranes [4]–[8]. Furthermore, by careful epitaxial growth techniques, strain can be introduced in these thin layers [5]–[8]. Strain changes mechanical properties, increases charge carrier mobility [9, 10], and affects subsequent self-assembly of quantum dots [11]. Upon etching of the oxide, strain engineered thin nanomembranes can be created with various shapes (including sheets, tubes, spirals, and ribbons) with thicknesses from several hundred nm to less than 10 nm [12]–[15].

Such membranes, consisting of the same materials as bulk Si-based semiconductors, can have unique properties related to their thinness, their shape, and the strain that is introduced via heteroepitaxy. These nanomembranes also are extremely flexible, while maintaining their perfect-single-crystal, dislocation-free nature. The electrical conductivity of Si nanomembranes (SiNMs), and, by extension, other very thin sheets, ribbons, and even wires of crystalline semiconductor materials, is especially interesting and can be quite different from their bulk counterpart because of the effect of interfaces. SOI typically has a top-Si (device layer) thickness of several hundred nanometres, and is bounded by SiO_2 both above and below. At a typical doping level of $10^{15}\,cm^{-3}$, the total number of dopants in $1\,cm^2$ of 100 nm thick membrane will be 10^{10}. At the same time there are of the order of $10^{11}\,cm^{-2}$ interface states at each oxide/Si interface that can trap charge, depleting the Si of mobile charge carriers. A 100 nm thick conventionally doped Si membrane should therefore behave as if it was intrinsic and not be able to conduct electricity at room temperature. As the membrane becomes thinner, the bulk doping concentration becomes increasingly irrelevant, because all charges are trapped at the interface. Yet under the proper circumstances, the membrane can conduct as well as bulk Si. This paper describes measurements, interpretations, and a discussion of potential impacts of conductivity in thin semiconductor nanomembranes.

The topic is relevant both scientifically and technologically. Measurements on thin semiconductor membranes, or any very thin semiconductor layer on an insulator, that depend on the flow of a current, such as scanning tunnelling microscopy (STM), Hall measurements, and electron emission and reflection processes (e.g., photoelectron spectroscopy and low-energy electron microscopy), become impossible if there is no conductivity. Similarly conduction through semiconductor quantum wires (for which there is typically a large surface-to-volume ratio) may be impossible if the surface traps and immobilizes dopant charges. In field effect transistors (FETs), it is, of course, always possible to invert the bands via an applied voltage to create a conducting channel, but voltages may need to be higher than desirable [16]. Technologically, one can imagine a range of nanosensors based on wires and membranes if conduction can be turned on or off via proper engineering of the band structure and distribution of charges in the nanostructure.

In semiconductor systems in which the conditions are such that all the free (bulk dopant) charge is trapped at the interfaces, it becomes essential to understand how these interfaces can be modified to create and control electrical conductivity. We describe in this paper how we understand electronic conduction in thin membranes of the Si system, using SOI as the

foundation. We measure conduction with STM and the van der Pauw four-point-probe method. We show that the π and π^* bands that are created by the dimer reconstruction on clean Si (001) and their position relative to the bulk bands of Si make possible room-temperature conduction in membranes of Si or SiGe, no matter how thin they are. If one surface of such a membrane is clean, these bands form with energy positions such that electrons can be thermally generated from the bulk valence band to the lowest-unoccupied molecular orbital (LUMO) band (the π^* band) of surface states. The result is conduction in nanomembranes with very high mobility. There is thus also a consequent high sensitivity to the surface condition, which affects the availability of states for thermal excitation. It follows logically that conductivity in the membrane can be tailored by surface chemistry. By tailoring the position of highest-occupied molecular orbital (HOMO) and LUMO bands of organic or inorganic atomic or molecular layers on the surface one facilitates thermal excitation of carriers between membrane 'bulk' and surface states to generate free carriers in the 'bulk' of the membrane and of the opposite sign in the surface states.

2. Membrane fabrication and van der Pauw resistance measurement

Membrane fabrication begins with the epitaxial growth of thin layers of SiGe and Si on top of ultra-thin SOI(001). Thicknesses and compositions of the layers can be adjusted according to the desired ultimate shape of the membrane and its properties. To achieve a flat sheet, we create a sandwich of Si–SiGe–Si with equal thicknesses of the Si layers to balance the strain after membrane release from the oxide. The membrane is released by selective chemical etching of the buried oxide layer using HF. Tensile strain will be induced in the Si layers of the membrane through *elastic* strain sharing between the Si layers and the compressively strained SiGe layer. After transfer to DI water, the membrane is completely released from the starting substrate and floats on the surface of the water, where it can be picked up by any new substrate that is not rapidly soluble in water. Finally hot plate annealing strengthens the bond between the released membrane and the new substrate. We have fabricated membranes larger than 1 cm^2 using this technique [7].

For the present study on conductivity, membranes that remained attached to the SOI substrate were used. A simple, thin layer of Si prepared by thinning the template layer in SOI (001) suffices to illustrate the conduction mechanism. We use SOI made by wafer bonding. The template layer, doped with boron nominally at 10^{15} cm^{-3} and initially 200 nm thick, was thinned to thicknesses ranging from 10 to 200 nm by dry thermal oxidation at 1050°C, followed by wet chemical etching to remove the oxide. The resulting Si membrane thickness was confirmed with ellipsometry. We measured the sheet resistance of these Si membranes, in contact with oxide on both sides (the buried oxide (BOX) below and a native oxide above) using the van der Pauw technique. We deliberately choose SOI with a thick buried-oxide layer (3 μm) to avoid any potential leakage current through the BOX to the underlying bulk Si. Ultra-thin SOI Si template layers are extremely resistive. The two Si–SiO_2 interfaces contain interface traps arising from structural or oxidation induced defects that are mainly in the form of Si dangling bonds [17, 18]. The two most important and intensely studied interface traps are the P_{b0} and P_{b1} defects, together producing a U-shaped distribution of energy states across the Si band gap [19, 20]. To understand how the oxide interface influences the measured sheet resistances, we employ a simple but well-established model for the interface states. We assume an interface density of states uniformly distributed through the band gap, with electronic properties acceptor-like in the upper half and donor-like in the lower

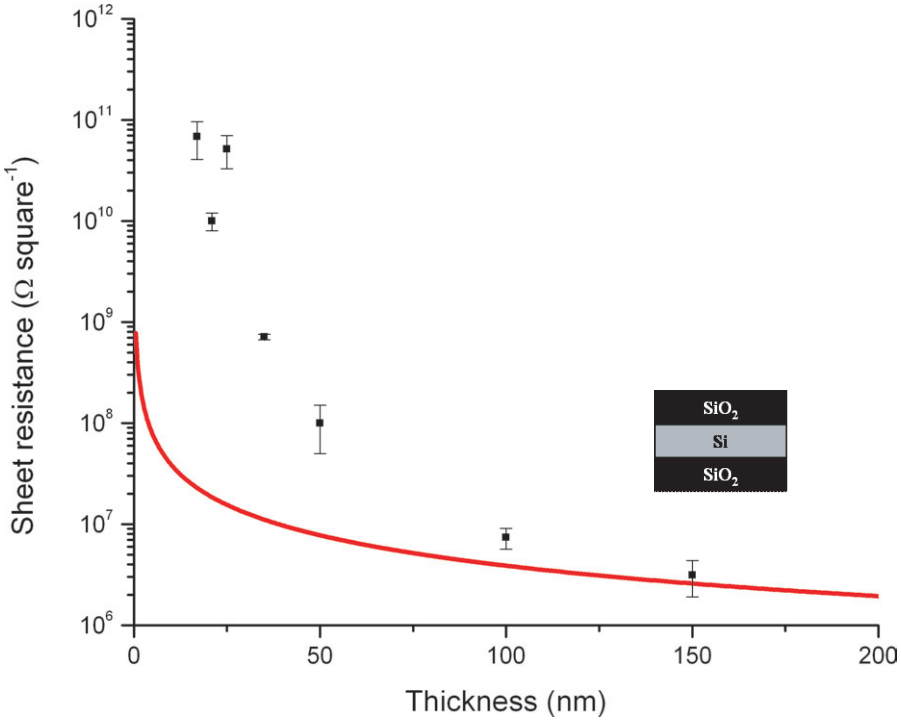

Figure 1. Sheet resistances of thin Si membranes bounded by two Si/SiO_2 interfaces, for different Si membrane thicknesses. Error bars (±S.D.) give the uncertainty in the measured sheet resistance values. The red curve is the calculation of sheet resistances at the nominal bulk doping level (boron, $10^{15}\,cm^{-3}$), assuming a uniform electron mobility of $\mu_e = 630\,cm^2\,Vs^{-1}$ and hole mobility of $\mu_h = 250\,cm^2\,Vs^{-1}$, values appropriate for thin films. The deviation of sheet resistances from the nominal values indicates that transport properties have been affected by Si/SiO_2 interfaces.

half of the band gap [16]. The acceptor type interface states are neutral when they are empty and negatively charged when filled; the donor type interface states are positively charged when they are empty and neutral when filled.

Figure 1 shows the measured sheet resistances for Si layers with different thicknesses. The red curve is the predicted sheet resistance calculated from the nominal doping level ($10^{15}\,cm^{-3}$) ignoring the interface states. In the calculation, we assume mobilities of $\mu_e = 630\,cm^2\,Vs^{-1}$ and $\mu_h = 250\,cm^2\,Vs^{-1}$ for electrons and holes respectively. Although mobilities of the 'bulk'-band carriers decrease abruptly when the film thickness is below 10 nm due to phonon scattering, interface roughness, and thin-film thickness fluctuations [21]–[23], they are relatively uniform for films with thicknesses ($\geqslant$10 nm) used in our experiments [24, 25] As observed in figure 1, when the film is thicker than 150 nm, sheet resistances approach the values calculated from the nominal bulk doping level. Below 150 nm all of the measured sheet resistances are greater than the nominal values calculated without considering interface states, and the thinner the film, the greater is the difference. For films thinner than 20 nm, sheet resistances approach those of intrinsic Si, a fact that indicates that the Fermi level has been pulled close to mid-gap.

This conduction behaviour in Si-based nanomembranes can be attributed to Si/SiO_2 interface properties. With the Si membrane layer boron doped at $10^{15}\,cm^{-3}$, the nominal position

of the Fermi level would be close to the valence band. However, those empty donor type interface states that are below the mid-gap but above the Fermi level will trap holes from the thin film and thus pull the Fermi level upward. For Si membranes thicker than ∼150 nm, conduction properties will be dominated by the bulk at this dopant concentration. For thinner Si membranes, because of the high interface states-to-bulk-dopant ratio, interfaces will play the dominant role and the Fermi level will be determined by a competition between interface trap density and membrane 'bulk' dopant concentration. As we have already indicated, a typical density of interface traps on the interface between thermally grown oxide and Si(001) is 10^{10}–10^{12} cm^{-2} eV^{-1} [18, 19], which is much higher than the areal density of dopants (10^9 cm^{-2}) in a, e.g., 10 nm membrane doped at 10^{15} cm^{-3}, and enough to deplete all the free carriers. We numerically fit the sheet resistances measured with the van der Pauw method to obtain the density of states of interface traps for our SOI samples. The values agree with those quoted here, as we show below.

The electronic nature and quality of the interfaces will determine the conductivity of a specific thickness of SiNM and influence measurements that depend on the flow of a current. For example, in STM, electrons will tunnel from tip to sample or vice versa, depending on the polarity of the voltage between tip and sample. To complete the circuit, current flows through the membrane (or along its surface) from right underneath the tip to the contact at the edge of the sample. Because a non-negligible current is necessary, STM typically can only image metal and semiconductor surfaces, and should not be able to image a SiNM that has the density of interface traps that ours do. Nevertheless, we obtain excellent STM images on ultra-thin bonded SOI(001), on SIMOX (implant with oxygen and anneal to form a buried oxide) SOI(001), and other forms of SOI, such as strained-SOI (sSOI)—all thin enough to eliminate conventional bulk conduction mechanisms. To explain this STM imaging, we identify a conduction mechanism associated with the surface, in the manner of a 'surface doping' [26].

3. STM measurements

For STM imaging, surfaces must be absolutely free of foreign atoms. Surface preparation of ultrathin SOI is challenging and requires great care. It consists of *ex situ* and *in situ* cleaning. *Ex situ*, the SOI was triple IMEC (Interuniversity Microelectronics center) cleaned [27]. A final piranha clean was performed to terminate the surface with a thin oxide layer for protection as the sample is transported to the ultrahigh vacuum (UHV) STM chamber. The base pressure of the chamber is below 1×10^{-10} Torr. Traditional *in-situ* preparation of bulk Si surfaces involves direct heating of the sample to 1500 K for several minutes. Such preparation is not possible for ultra-thin SOI, because the Si template layer will dewet and agglomerate into 3D Si islands when annealed at high temperatures in UHV, as Si on SiO_2 is not thermodynamically stable, in contrast to the inverse [28]–[30]. An example of an ultrathin SOI sample in which the 9 nm Si template layer dewetted from the oxide and agglomerated after annealing at 900°C in UHV for several minutes is shown in figure 2. To avoid dewetting and agglomeration, we use an alternative approach that allows us to clean the Si surface *in situ* at low temperatures. We slowly (∼0.5 ML min^{-1}) deposit several monolayers of Si or Ge at 700°C. The surface oxide is removed by reduction with Si or Ge through the reactions

$$SiO_2 + Si \rightarrow 2SiO$$

$$SiO_2 + Ge \rightarrow SiO + GeO.$$

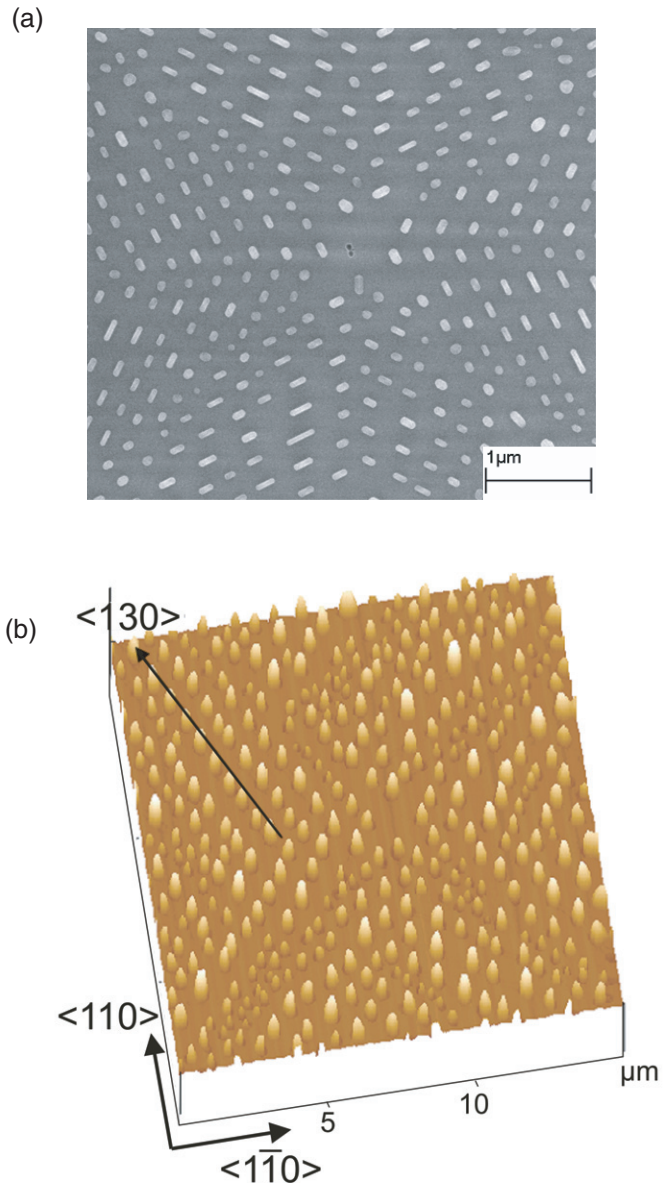

Figure 2. Dewetting and agglomeration of a 9 nm Si template layer on SOI(001) annealed at 900°C for several minutes in UHV. The continuous Si layer has broken up into isolated Si islands sitting on SiO_2. Panels (a) and (b) are SEM and AFM images of the sample respectively. The agglomeration pattern shows a 4-fold symmetry and islands ordering along ⟨130⟩ directions [29].

SiO and GeO produced by these reactions are volatile at temperatures above 500°C for SiO [31, 32] and 360°C for GeO [33]. Finally, we anneal the sample at 800°C (still below the critical temperature for agglomeration) for 2 min, anneal it at 600°C for 30 min, radiation cool it to room temperature, and transfer it to the STM station. We are able to produce nearly defect-free surfaces with this cleaning procedure. Our low-thermal-budget surface cleaning method allows us to remove the protective oxide and image the surface with STM and perform other

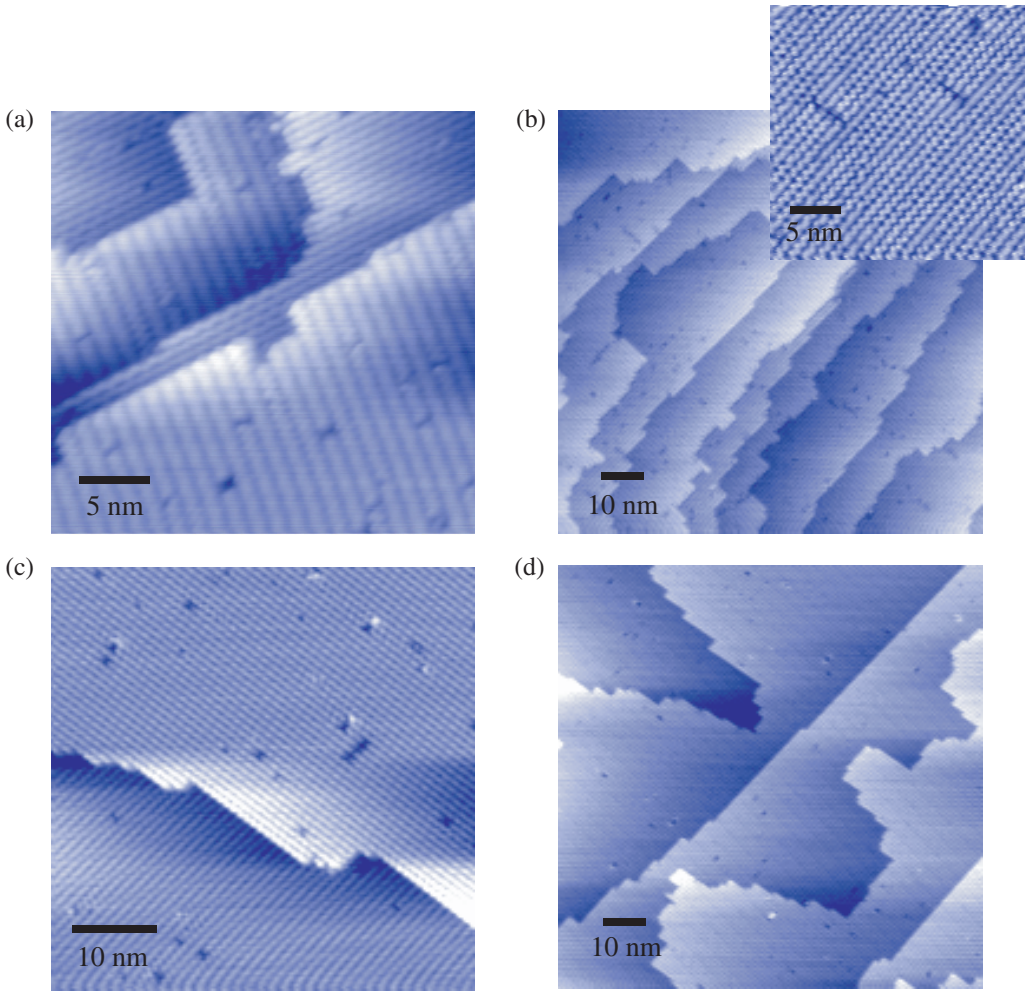

Figure 3. STM images of different types of SOI. (a) Filled-state image of a 10 nm thick Si membrane in wafer-bonded SOI(001) with the top oxide removed by several monolayers of Si. (b) Same as (a) but using several monolayers of Ge to remove the oxide. Inset, filled-state image showing dimer zigzag buckling caused by a submonolayer of Ge on the surface. (c) Filled-state image of a 20 nm Si layer in SIMOX SOI(001). (d) Filled-state image of a 15 nm strained-Si layer in sSOI(001) (0.8% tensile strain).

charge-transport-dependent measurements without destroying the fragile Si template layer. Low-thermal-budget cleaning is also required in the fabrication of ultrathin-body (UTB) FETs to prepare the surface for the subsequent growth of epitaxial layers for raised source and drain. We believe the above surface preparation method should be applicable to actual device fabrication, because the same deposition technique and source material can be used both to clean the substrate and to grow epitaxial layers.

Figure 3 shows STM images taken on several types of SOI samples. The images were acquired at room temperature in the constant-current mode using a tunnelling current of 0.1 nA. Filled-state images of the Si template layer surface were obtained at tip biases of −2 V relative to the sample. Figures 3(a) and (b) show bonded SOI(001) surfaces with the oxide removed by 3 ML

of Si and 3 ML of Ge, respectively. The Si membrane (i.e., template layer) thickness is 10 nm. The images are comparable to those obtained from a bulk Si(001) surface [34]. The clean Si surface of SOI(001) reconstructs to form rows of dimerized atoms, just as does bulk Si(001) [35]. The intrinsic anisotropic stress (tensile along the dimer bonds; compressive along the dimer rows) leads to alternate orthogonal (2 × 1) and (1 × 2) terraces on the surface, terminated respectively by S_B and S_A steps [36].

The surface obtained using Ge to remove the native oxide is subtly different from that obtained using Si to remove the native oxide or to the bulk-Si(001) surface cleaned in the standard manner (flash heating). It shows a dimer buckling zigzag pattern on the surface (insert of figure 3(b)) resulting from intermixing of Ge into the Si surface [37]. The amount of Ge present is clearly much less than 1 ML, because we do not observe dimer vacancy lines that begin to form at concentrations of Ge higher than several tenths of a monolayer [38, 39]. As shown in figure 3(c), SIMOX SOI samples can be imaged as well as bonded SOI, even though the density of traps at the Si/BOX interface in SIMOX SOI is generally higher than the interface trap density in wafer-bonded SOI [40]. Finally, we have imaged 15 nm thick membranes of 0.8% tensile sSOI, as shown in figure 3(d). Sawtooth structured S_B steps are observed on the surface, a sign of the surface of strained Si, for example, Si films epitaxially grown on SiGe layers [41].

As we have discussed above, STM requires at least some conductivity of the substrate. However, ultrathin Si membranes (attached or released) that are terminated by oxide on both surfaces are highly resistive and act like intrinsic Si, as we measured with the van der Pauw technique. The sheet resistance of a 20 nm thick Si membrane is $\rho_{2D} = 80\,\mathrm{G\Omega\,square^{-1}}$. Of course, we image with the oxide on the front surface removed. Even with the top oxide removed, the Si–SiO_2 interface states at the back surface of a 20 nm membrane with the lowest possible interface state density are sufficient to deplete the membrane fully of free carriers (this is also why the SIMOX samples do not behave differently), and thus removal of the oxide from one face will not measurably lower the nanomembrane sheet resistance. The Si membrane bulk, without any other source of carriers, thus remains highly resistive after removal of the top oxide. If the electrical contact is far from the STM tip, as is the case in our experiments, we can approximate the sample resistance R as the resistance between two concentric circles of radii r_1 and r_2, with $r_2 \gg r_1$:

$$R = \int_{r_1}^{r_2} \rho_{2D} \frac{\mathrm{d}r}{2\pi r} = \frac{\rho_{2D}}{2\pi} \ln\left(\frac{r_2}{r_1}\right).$$

For $r_1 \sim 1$ nm and $r_2 \sim 0.5$ cm, we find that $R \approx 2.5\rho_{2D} = 200\,\mathrm{G\Omega}$, which is far larger than the total circuit resistance (20 GΩ) in our STM set up and thus no imaging should be possible.

As we suggested, the SiNM is intrinsic because the bottom Si/BOX interface binds all the dopant-produced free carriers (for our sample the unsaturated donor type interface states trap holes from the Si membrane, leading to a positively charged Si/BOX interface). To explain the ability to image with STM requires a new conduction mechanism. To minimize the dangling bonds on the surface, Si surface atoms reconstruct to form dimers that are tilted. Charge transfer inside the tilted dimers results in an empty π^* band and a filled π band, each with the density of states of about $10^{15}\,\mathrm{cm^{-2}\,eV^{-1}}$. The observed 2 × 1 and 1 × 2 surface reconstructions at room temperature are thought actually to be c(4 × 2) and c(2 × 4) reconstructions, where the increased unit mesh size is caused by tilted dimers, which, however, move so rapidly that the STM sees the lower symmetry [42, 43]. The surface electronic structure of the c(4 × 2) reconstruction has

been calculated from first principles [44]. The gap of about 0.5 eV between the π^* (LUMO) and π (HOMO) bands is positioned about the Si valence band edge, with the bottom of the π^* band approx. 0.35 eV above the Si valence band maximum (VBM) [44]. The calculated surface band gap and the position of the π^* band are supported by STS and optical absorption experiments [45]–[48]. A recent two-photon photoemission experiment suggests a larger surface band gap and a separation of approx. 0.6 eV between the surface π^* band and the Si VBM [49, 50]. We use this range of values in our numerical calculation. We use a position of the surface π band 0.15 eV below the Si VBM, inferred from both theory and experiment.

For intrinsic Si at room temperature, it would be very difficult to excite electrons thermally from the Si valence band to the Si conduction band because of the 1.1 eV band gap, but it is much easier to excite electrons from the bulk Si valence band, across the reduced gap to the surface π^* states. As a result of this thermal generation process, electrons and holes will respectively populate the surface states and the bulk-Si valence band. Two parallel conducting paths, electrons on the surface and holes in the 'bulk' of the Si membrane, can now contribute to the conductivity of the membrane system. The effective resistance will be

$$\frac{1}{R_{\mathrm{eff}}} = \frac{1}{R'_{\mathrm{bulk}}} + \frac{1}{R_{\mathrm{surface}}}.$$

We assume that the hopping conduction of charge at the Si–Si dioxide interface is negligible in comparison to these two paths. We will demonstrate that this assumption is good.

4. Numerical calculation

The electronic band structures of SiNMs bounded by two Si/SiO_2 interfaces and by one Si/SiO_2 interface and a clean surface are shown in figure 4. The band bending in ultrathin Si membranes has been grossly exaggerated in the band diagrams. To achieve a better understanding of the change of electronic properties of the Si membrane before and after the introduction of a clean surface, we also perform numerical calculations for both situations by solving Poisson's equations with appropriate boundary conditions. In the direction normal to the interface, there is no current flow: both the electron and hole current density components in this direction, J_{n} and J_{p} respectively, are equal to zero. As a result, from the definition of the current components, we obtain the electron and hole densities

$$\begin{aligned} J_{\mathrm{n}} &= n(x)e\mu_{\mathrm{n}}F(x) + eD_{\mathrm{n}}\frac{\mathrm{d}n(x)}{\mathrm{d}x} = 0 \Rightarrow n(x) = n(0)\exp\left(-\int_0^x \frac{eF(x)\,\mathrm{d}x}{k_{\mathrm{B}}T}\right), \\ J_{\mathrm{p}} &= p(x)e\mu_{\mathrm{p}}F(x) - eD_{\mathrm{p}}\frac{\mathrm{d}p(x)}{\mathrm{d}x} = 0 \Rightarrow p(x) = p(0)\exp\left(\int_0^x \frac{eF(x)\,\mathrm{d}x}{k_{\mathrm{B}}T}\right), \end{aligned} \tag{1}$$

where x is the direction normal to the interface, originating at the buried-oxide interface, p and n are the hole and electron densities, respectively, while $\mu_{\mathrm{p/n}}$ and $D_{\mathrm{p/n}} = \mu_{\mathrm{p/n}}k_{\mathbf{B}}T/e$ are the hole/electron mobility and diffusion constant, respectively. F is the electric field in the x-direction, related to the variation of the intrinsic Fermi level E_{i} via $eF = \mathrm{d}E_{\mathrm{i}}/\mathrm{d}x$. So we can

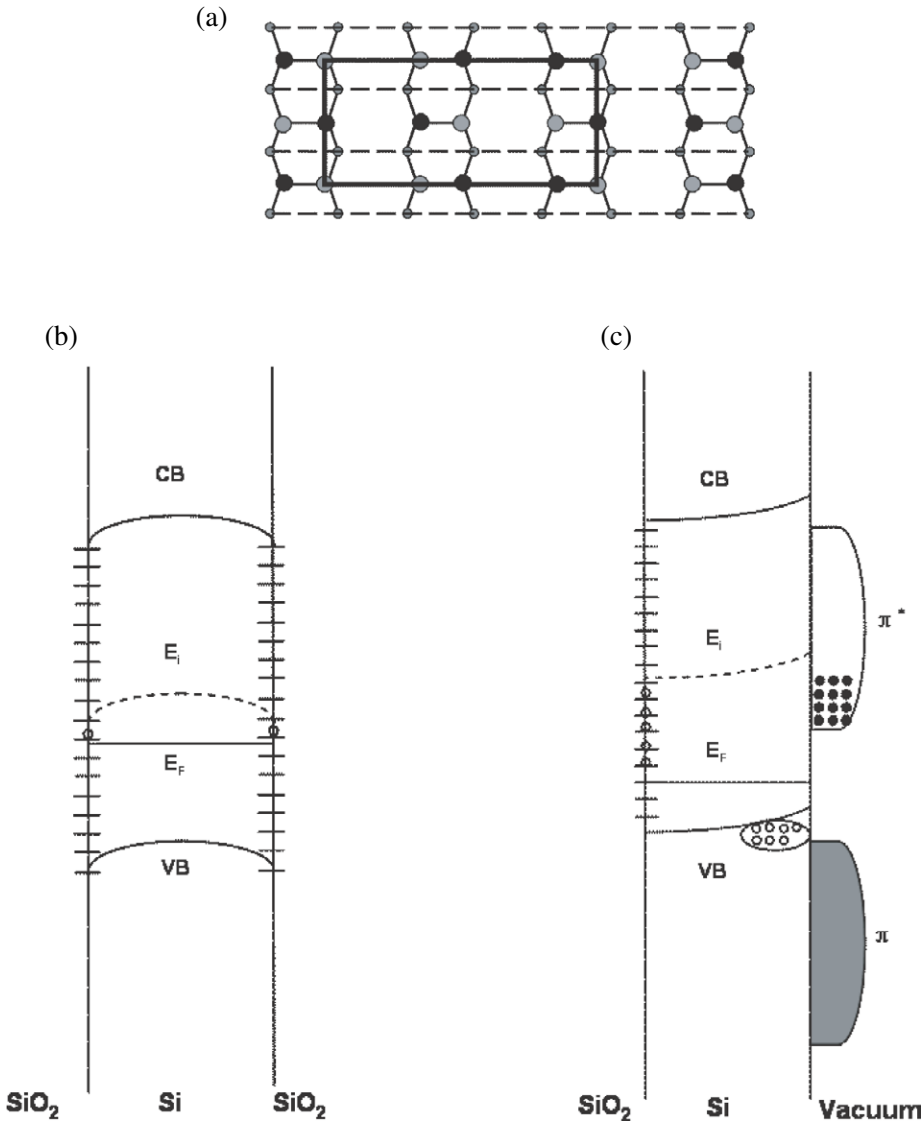

Figure 4. Proposed band diagrams showing interface, bulk, and surface bands for a thin Si membrane and for the surface π^* band 0.35 eV above the bulk VBM. (a) Schematic diagram of the C(4 × 2) reconstruction on clean Si(001). (b) SiNM bounded by two Si/SiO_2 interfaces. For a 10 nm Si film, the maximum band bending is $<100\,\mu$ eV (grossly exaggerated in the figure). The Fermi level is ∼25meV below the midgap. (c) SiNM bounded by C(4 × 2) reconstructed Si(001) on one face. The existence of the surface bands results in a reduced effective bandgap (∼0.35eV in this example) between the bulk VBM of the SiNM and the bottom of the surface π^* band. The enhanced conductivity is derived from the thermal population of carriers in those bands. For a 10 nm SiNM, the maximum band bending is approx. 7 meV. The Fermi level is approx. 0.4 eV below the midgap. CB, conduction band; VB, valence band; E_F, Fermi level; E_i, intrinsic level (midgap level). Short lines denote the interface trap states. Holes are indicated by '○'open circles and electrons are indicated by '●' filled circles.

write

$$n(x) = n(0)\exp\left(-\frac{E_{\rm i}(x) - E_{\rm i}(0)}{k_{\rm B}T}\right) = n_{\rm i}\exp\left(-\frac{E_{\rm i}(x) - E_{\rm F}}{k_{\rm B}T}\right),$$

$$p(x) = p(0)\exp\left(\frac{E_{\rm i}(x) - E_{\rm i}(0)}{k_{\rm B}T}\right) = n_{\rm i}\exp\left(\frac{E_{\rm i}(x) - E_{\rm F}}{k_{\rm B}T}\right),$$

where $E_{\rm F}$ is the position of the Fermi level in the x direction, and n_i is the intrinsic carrier density in bulk Si ($n_{\rm i} = 10^{10}\,{\rm cm}^{-3}$ at room temperature). By using Gauss's law ${\rm d}F/{\rm d}x = e[p(x) - n(x) - N_{\rm A}]/\varepsilon\varepsilon_0$, where $N_{\rm A}$ is the uniform acceptor doping throughout the sample and $\varepsilon = 11.8$ is the Si dielectric constant, accompanied by the transformation ${\rm d}^2E_{\rm i}/{\rm d}x^2 = (1/2)({\rm d}/{\rm d}E_{\rm i})({\rm d}E_{\rm i}/{\rm d}x)^2$, we obtain an equation describing the spatial variation of the intrinsic Fermi level (valence and conduction bands follow the same shape) between the two interfaces

$$\frac{\rm d}{{\rm d}E_{\rm i}}\left(\frac{{\rm d}E_{\rm i}}{{\rm d}x}\right)^2 = \frac{2e^2}{\varepsilon\varepsilon_0}\left\{n_{\rm i}\exp\left[\frac{E_{\rm i}(x) - E_{\rm F}}{k_{\rm B}T}\right] - n_{\rm i}\exp\left[-\frac{E_{\rm i}(x) - E_{\rm F}}{k_{\rm B}T}\right] - N_A\right\}. \tag{2}$$

Equation (2) is simply a variant of Poisson's equation. For simplicity, we will introduce the reduced quantities $\xi(x) = [E_{\rm i}(x) - E_{\rm F}]/k_{\rm B}T$, $\nu = N_{\rm A}/n_{\rm i}$, and the intrinsic Debye length $L_{\rm Di} = \sqrt{\varepsilon\varepsilon_0 k_{\rm B}T/2e^2n_{\rm i}}$. As a result, equation (2) can be integrated to yield the central equation, which we will be solving numerically

$$\dot{\xi}^2 = {\rm const.} + \frac{1}{L_{\rm Di}^2}[\exp(\xi) + \exp(-\xi) - \nu\xi], \quad \left(\dot{\xi} \equiv \frac{{\rm d}\xi}{{\rm d}x}\right). \tag{3}$$

Consider first a Si membrane of thickness L, sandwiched between two Si/SiO_2 interfaces. Because of the nature of the formation of the interface states [18], the interface is charge-neutral if the Fermi level crosses it at midgap [16]. We will assume that both interfaces in our samples have the same distribution of states, and the sheet density of the charge trapped at the interface will be proportional to the difference between the intrinsic level and the Fermi level at the interface:

$$Q_{\rm it}(x_{\rm interface}) = eD_{\rm it}[E_{\rm i}(x_{\rm interface}) - E_{\rm F}], \quad x_{\rm interface} = 0 \text{ or } L. \tag{4}$$

Because the interfaces have the same trap density of states, the bands have to be symmetric about $x = L/2$, so we only need to treat one half of the film thickness. Also, the electric field is anti-symmetric about $L/2$, $\dot{\xi}(L/2 - x) = -\dot{\xi}(L/2 + x)$, so

$$\dot{\xi}(L/2) = 0, \tag{5}$$

which is our first boundary condition. From (4) and Gauss's law at $x = 0$, $Q_{\rm it}(0)/\varepsilon\varepsilon_0 = F(0)$, we obtain our second boundary condition

$$\dot{\xi}(0) = \frac{e^2 D_{\rm it}}{\varepsilon\varepsilon_0}\xi(0). \tag{6}$$

The Si membrane is initially p-type doped, so with the introduction of the trap levels, the holes flee towards the interfaces, leaving the interfaces positively charged and the membrane negatively

charged. As a result, we expect the electric field to be positive for $0 < x < L/2$ (and negative for $L/2 < x < L$).

Consequently, upon incorporation of (5) into (3), we obtain the equation that is to be integrated numerically on the interval $0 < x < L/2$:

$$\dot{\xi} = +\frac{1}{L_{Di}}\sqrt{\exp(\xi) + \exp(-\xi) - \nu\xi - \exp\left[\xi(L/2)\right] - \exp\left[-\xi(L/2)\right] + \nu\xi(L/2)}, \tag{7a}$$

with the boundary condition

$$\left(\frac{e^2 D_{\mathrm{it}} L_{\mathrm{Di}}}{\varepsilon\varepsilon_0}\right)^2 \xi(0)^2 = \exp\left[\xi(0)\right] + \exp\left[-\xi(0)\right] - \nu\xi(0) - \exp\left[\xi(L/2)\right] - \exp\left[-\xi(L/2)\right] + \nu\xi(L/2). \tag{7b}$$

In the numerical solution to (7*a*), $\xi(L/2)$ is swept until, after backward integration from $L/2$ to 0, the boundary condition (7*b*) is satisfied. It should be noted that the procedure above is not restricted to two interfaces with the same interface trap density of states. In the case of different trap densities at the two interfaces, the two boundary conditions are equation (6) and an equivalent one at the other interface (with an extra minus sign).

If one of the Si/SiO_2 interfaces is removed and replaced by a clean reconstructed surface, one still needs to solve equation (3); however, boundary condition (5) no longer holds. Similar to the case of two different interface trap densities, the problem is no longer symmetric around $x = L/2$. A major difference now is that the π^* surface band introduces a high density of available electronic states in the Si bandgap, acting therefore as a sink for electrons. In the case of two Si/SiO_2 interfaces, both interfaces were positively charged, while in the case of one interface and a surface, the surface band sucks electrons away and becomes negatively charged, leaving excess holes to be distributed between the interface states and the membrane.

Under the assumption that the Fermi level is not too close (within $3k_BT$) to the bottom of the π^* band, the sheet density of electrons n_S at the surface can be calculated according to

$$n_S = \int_{E^*_{\min}}^{E^*_{\max}} D_S f(E)\,\mathrm{d}E \approx \int_{E^*_{\min}}^{E^*_{\max}} D_S \exp\left(-\frac{E - E_F}{k_BT}\right)\mathrm{d}E = D_S k_B T \exp\left(-\frac{E^*_{\min} - E_F}{k_BT}\right), \tag{8a}$$

where D_S, the density of states in the π^* band, is assumed constant, and $E^*_{\max}$, $E^*_{\min}$ denote the top and bottom energies of the π^* band, respectively. The last equality in (8*a*) was obtained by noting that the width of the π^* band $(E^*_{\max} - E^*_{\min}) \approx 700\,\mathrm{meV}$ greatly exceeds k_BT at room temperature (26 meV). In a similar fashion, the number of holes in the π band can be calculated as

$$p_S = \int_{E_{\min}}^{E_{\max}} D_S[1 - f(E)]\,\mathrm{d}E \approx D_S k_B T \exp\left(\frac{E_{\max} - E_F}{k_BT}\right), \tag{8b}$$

where $E_{\max}$, $E_{\min}$ denote the top and bottom energy of the π band, respectively. We see that n_S and p_S satisfy a relationship similar to what one is used to seeing in bulk

$$n_S p_S = (D_S k_B T)^2 \exp\left(-\frac{E^S_G}{k_BT}\right), \tag{9}$$

where $E^S_G = E^*_{\min} - E_{\max}$ is the surface gap between the π^* and π bands.

From Gauss's law, at the surface

$$F(L^-) = \frac{e(n_S - p_S)}{\varepsilon\varepsilon_0} = \frac{eD_S k_B T}{\varepsilon\varepsilon_0}\left[\exp\left(\frac{E_F - E^*_{min}(L)}{k_B T}\right) - \exp\left(\frac{E_{max}(L) - E_F}{k_B T}\right)\right].$$

After noting the exact positions of the edges of the π and π^* bands with respect to the bulk conduction and valence bands [44], we obtain the new boundary condition

$$\dot{\xi}(L) = \frac{e^2 D_S}{\varepsilon\varepsilon_0}\left\{\exp\left[\frac{E_i(L) - E^*_{min}(L)}{k_B T} - \xi(L)\right] - \exp\left[\frac{E_{max}(L) - E_i(L)}{k_B T} + \xi(L)\right]\right\}. \quad (10)$$

In contrast to the case of a Si membrane between two Si/SiO_2 interfaces, the electric field (and consequently $\dot{\xi}$) does not change sign: it remains positive throughout the film. As a result, we can take the positive sign of the square root of equation (3), and obtain the following equation

$$\dot{\xi} = \sqrt{\text{const.} + \frac{1}{L^2_{Di}}[\exp(\xi) + \exp(-\xi) - \nu\xi]}, \quad (11)$$

accompanied by the boundary conditions (6) and (10).

In our numerical calculation, shown in figure 5(a), we first fit the resistances obtained from our van der Pauw measurements of SiNMs of different thicknesses with two Si/SiO_2 interfaces with an interface density of states; for this configuration, we also consider the contribution of hopping conduction of the charge at the Si/SiO_2 interface, which occurs in parallel with 'bulk' conduction. We give the interface hopping mobility a reasonably large range: 0 to 1 $cm^2\,Vs^{-1}$ for fitting [51]. The shapes of the curves in figure 5(a) are primarily determined by the interface trap density, as it determines how quickly the Fermi level moves towards midgap. The interface hopping conduction serves largely to shift the curve up and down. Figure 5(a) shows that the numerical model fits the data quite well, providing an interface trap density of $10^{10}\,cm^{-2}\,eV^{-1}$ and interface hopping mobility of 0 $cm^2\,Vs^{-1}$. The latter result means that carriers at the Si/SiO_2 interface are effectively immobile (we have not been able to find independent estimates of this conductivity). Using the fitted interface trap density from our resistance measurements, we have calculated the sheet resistance of membranes terminated by vacuum on one side, as shown in figure 5(b). Because of the appropriately positioned surface states, additional free carriers can be created via excitation of electrons from the valence band of SiNMs into the surface π^* band at room temperature or below. The conductivity of SiNMs decreases with the increase of bandgap between the surface π^* band and the Si VBM. Nevertheless, conductivities of SiNMs are significantly enhanced by the introduction of surface bands for the whole range of values of this bandgap proposed in the literature, and are several orders of magnitude higher than those of SiNMs bounded by two oxide interfaces. For the conventional doping concentration we have here, the bulk doping level is virtually irrelevant for both the oxide- and the vacuum-terminated Si membranes, up to thicknesses above 100 nm. For a 20 nm Si membrane the doping would have to be in the bulk degenerate region for it to be relevant to conduction.

Figure 5(b) also shows the potential influence of surface charge carrier mobility. The π^* surface state electrons on Si(001) disperse preferentially along the dimer row direction [44]. The effective mass of surface electrons is estimated to be $0.28m_0$ (m_0 corresponds to the

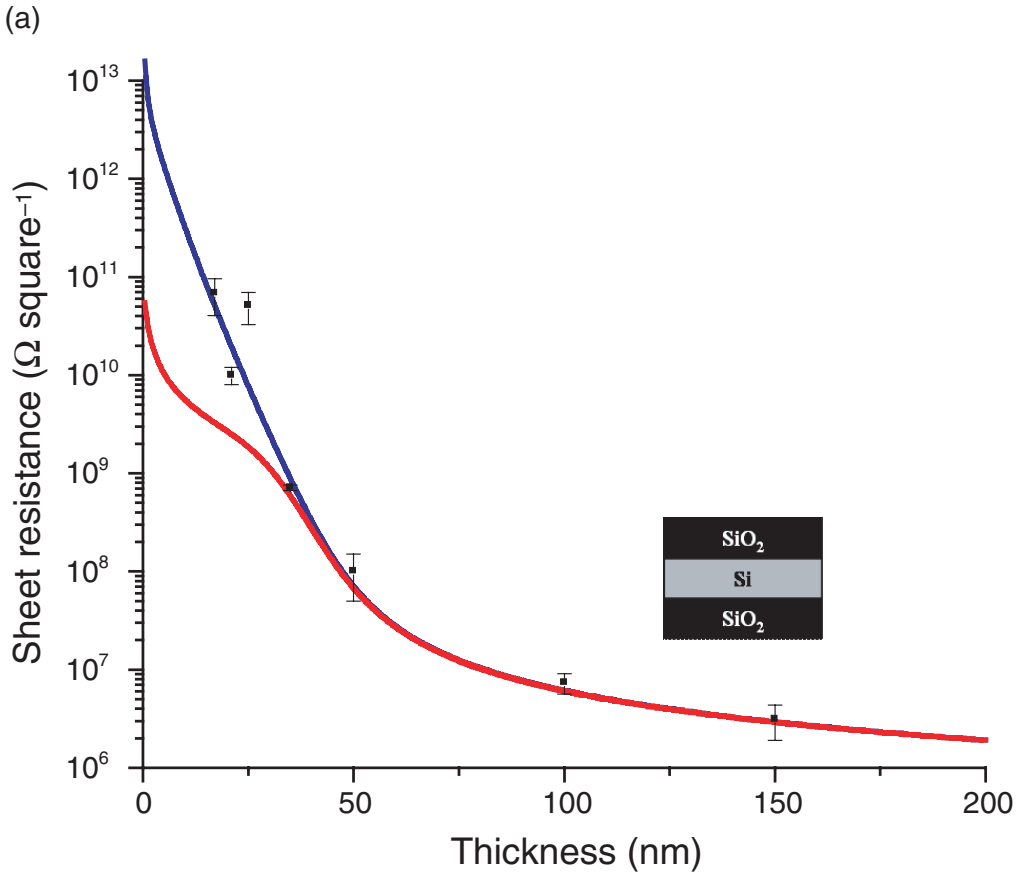

Figure 5. Numerical calculation of the SiNM sheet resistances for both oxide- and vacuum-terminated surfaces. (a) Numerical fits to the van der Pauw resistance measurements. The blue curve uses an interface hopping mobility of $0\,\mathrm{cm^2\,Vs^{-1}}$, the red curve $1\,\mathrm{cm^2\,Vs^{-1}}$, both with an interface trap density of states $D_{\mathrm{it}} = 10^{10}\,\mathrm{cm^{-2}\,eV^{-1}}$. van der Pauw resistances can fit well with the blue curve, which indicates that the hopping mobility on Si/SiO_2 interfaces is negligible.

free-electron mass) from the dispersion relation derived from standing-wave patterns observed with low-temperature STM along Si dimer rows when Al is adsorbed on the surface [52, 53]. Because of electron scattering by steps and defects on the surface, the surface electron mobility is likely to be small relative to the high mobility of holes in the 'bulk' of the membrane. Attempts have been made to measure the surface conductance of Si(111) and Si(001) using low-temperature STM [54], microscopic four-point probe methods [55, 56], or macroscopic van der Pauw measurements [57]. It is not possible in any of these experiments to measure directly the surface-state conductivity, because the surface is always electrically 'in contact' with the underlying bulk. For example, in Si(111) 7×7, the deduced surface-state conductance from various measurements ranges from 10^{-4} [57] to $10^{-9}\,\Omega^{-1}$ square^{-1} [54], while the conductivity of Si(001) (2×1) determined from macroscopic van der Pauw measurements is of the order of $10^{-6}\,\Omega^{-1}$ square^{-1} [57]. Ultimately, although we have not yet done these measurements, the proper way to measure surface conductivity and mobility is with membranes, which can be made

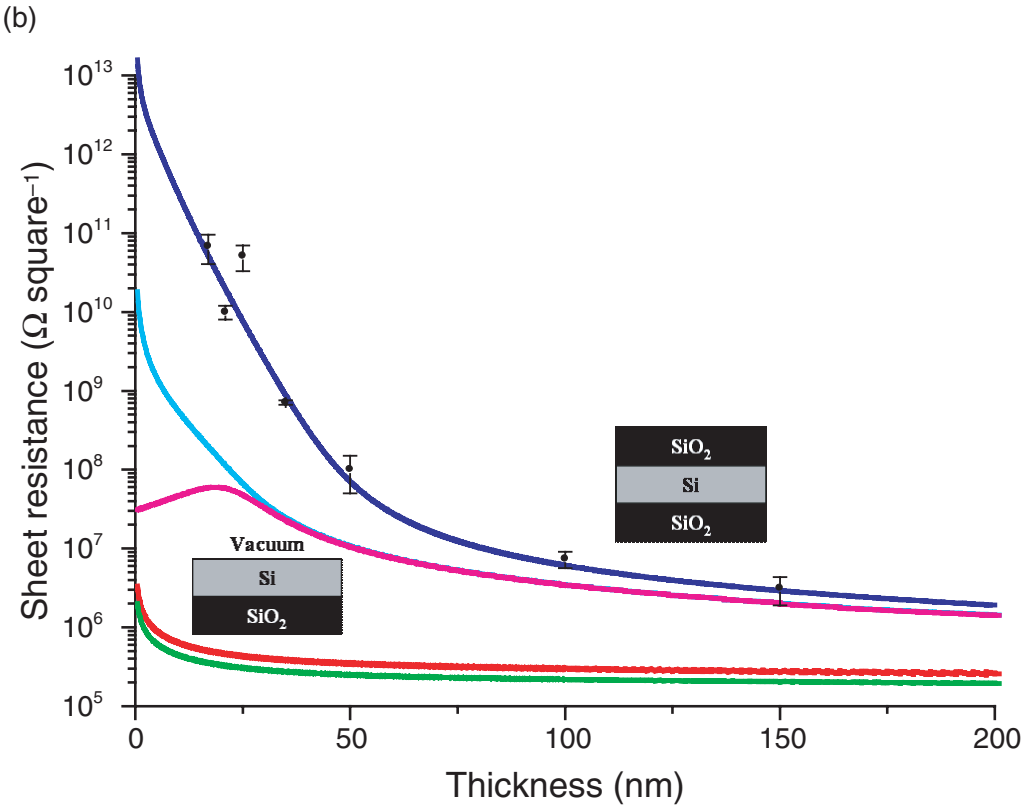

Figure 5 (continued). (b) Numerical calculation of the SiNM sheet resistance to a vacuum-terminated surface using the same D_{it}. The cyan and magenta curves assume that the bottom of the surface π^* band is positioned approx. 0.6 eV above the Si VBM, with negligible surface electron mobility of the cyan curve and 100 $cm^2\,Vs^{-1}$ for the magenta curve. The red and green curves assume a 0.35 eV bandgap between the surface π^* band and Si VBM. The red curve corresponds to a negligible surface electron mobility, and green curve for the surface electron mobility of 100 $cm^2\,Vs^{-1}$. For very thin SiNMs, the existence of appropriate surface bands leads in all cases to a conductivity dramatically higher than a SiNM with two oxide terminations.

totally intrinsic, as we have shown. For present purposes, how well the surface states can conduct does not really matter to our argument that carriers are created by a surface doping mechanism. In SOI(001) the holes created in the bulk valence band by electrons that are thermally excited at room temperature to the surface state are sufficient to provide the conductivity for STM experiment, regardless of the surface electron mobility, as figure 5(b) shows. Hence, the surface π^* band could act like a parking lot for electrons (zero mobility) that are thermally excited from the 'bulk' membrane valence band. Alternatively, the surface can conduct at very high values and not change the basic picture.

Other choices for providing empty states (or filled states if using the 'bulk' conduction band) at appropriate energies relative to the 'bulk' membrane bands are, of course, possible via adsorption or film growth.

5. Discussion and conclusion

On the basis of this analysis, we expect that STM imaging will always be possible on SOI(001), no matter how thin the Si template layer or whether it is bulk depleted. Furthermore in any material that has surface bands (e.g., also Si(111)), considerations of bulk depletion become irrelevant for thin enough membranes if surface states with appropriate band positions and density of states are present. For materials that do not have surface bands in the bulk band gap, such as cleaved GaAs (110), measurements that depend on electron transport that are possible in the bulk material may fail for thin enough films or membranes, because interface and surface localized trap states deplete all carriers.

We predict that disruption of clean-surface bands by chemisorption of selective elements or by sufficient disorder will reduce or eliminate the conductivity of thin SiNMs (and thus also eliminate the ability to image the surface or to perform other measurements that depend on electron transport). So, for example, termination of the surface with hydrogen [58] or halogen [59] will suppress the surface states and prevent the generation of free carriers in the membrane and thus STM imaging. The prediction on required surface quality also impacts the two earlier STM studies on SOI(001) that have been reported [60, 61]. Both demonstrated difficulty in STM imaging of SOI all with about the same bulk doping level as we have used. Lin *et al* [60] could not image SIMOX SOI(001) with a 35 nm Si template layer thickness, but could image a layer that was much thicker (170 nm thick). Sutter *et al* [61] could not image 10 nm Si template layers on SIMOX SOI(001), but could do so after depositing around 10 ML of Si buffer followed by 1.2 ML of Ge. Both reports invoked bulk depletion as the cause of their inability to image. We show here that it is possible to image much thinner layers with this bulk doping level. The surface quality, and not the degree of the bulk depletion of the Si template layer, ultimately determines the conductivity of the membrane.

Clean-surface states of Si(001) can be preserved outside vacuum using approaches that leave the surface chemically protected, but preserve the dimer structure and the high density of surface states [62]–[64]. Such surfaces should have the same conductivity enhancement as we describe above. Organic molecules covalently bound to Si can be chemically and thermally stable. Tailoring the position of HOMO and LUMO bands of such organic molecules relative to the 'bulk' Si bands maintains the ability for thermal generation of free carriers in the membrane. Either electrons or holes can be thermally generated, depending on the exact positions of the HOMO and LUMO bands relative to the Si membrane conduction and valence band edges. The addition of such layers provides a potentially practical approach to manufacture nanoscale sensor devices. The idea of 'surface doping' can be applied in chemical- or biological-sensor technology by monitoring the electronic conductivity of chemically functionalized SiNMs in different chemical environments. Meanwhile, inducing free carriers without dopants may give an alternative solution for the problem of dopant fluctuation in nanoscale devices [65]. Furthermore, carrier mobilities in membranes can be improved by eliminating the scattering at dopants.

In summary, we describe surprising electronic conductivity in very thin SiNMs in terms of a 'surface doping' mechanism. We show that STM imaging of the clean surface of SOI(001) with nominal doping levels of 10^{15} cm^{-3} and Si template layers as thin as 10 nm is entirely possible, even though such membranes are bulk-depleted. The conduction occurs via free carriers generated by thermal excitation into surface bands from the membrane bulk valence band. We predict that only disruption of the surface bands can hinder conductivity in the thin top layer of SOI(001), no matter how thin the membrane is or how low the bulk doping level is. Such disruption can come

via surface disorder or chemisorption that breaks the pi-bonded dimer chains that produce the surface bands. In systems that do not have surface bands, we predict that making the layer thin enough to cause bulk depletion will inhibit conductivity of the film. The conducting mechanism is not unique to the Si(001)c(4 × 2) [(2 × 1)] surface configuration. Any surface 'termination' that provides energy levels close to the Si band edges to accept or donate electrons should suffice. Manipulating surface chemistry to control the film conductivity can be achieved by terminating the surface with molecular species that have appropriate HOMO and LUMO levels.

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