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# Electronic transport in nanometre-scale silicon-on-insulator membranes

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**The widely used 'silicon-on-insulator' (SOI) system consists of a layer of single-crystalline silicon supported on a silicon dioxide substrate. When this silicon layer (the template layer) is very thin, the assumption that an effectively infinite number of atoms contributes to its physical properties no longer applies, and new electronic, mechanical and thermodynamic phenomena arise[1–4], distinct from those of bulk silicon. The development of unusual electronic properties with decreasing layer thickness is particularly important for silicon microelectronic devices, in which (001)-oriented SOI is often used[5–7]. Here we show—using scanning tunnelling microscopy, electronic transport measurements, and theory—that electronic conduction in thin SOI(001) is determined not by bulk dopants but by the interaction of surface or interface electronic energy levels with the 'bulk' band structure of the thin silicon template layer. This interaction enables high-mobility carrier conduction in nanometre-scale SOI; conduction in even the thinnest membranes or layers of Si(001) is therefore possible, independent of any considerations of bulk doping, provided that the proper surface or interface states are available to enable the thermal excitation of 'bulk' carriers in the silicon layer.**

The use of SOI in microelectronics and nanoelectromechanical systems is already pervasive. SOI promises, in fact, to become the platform for future high-speed electronics as well as for a range of sensor technologies[5,7]. Many of the expected advances will depend on making the Si template layer in SOI increasingly thin. In terms of electronic-transport properties, such very thin crystalline layers pose unique challenges. When the Si layer becomes thin enough, charge traps at the oxide/Si interface will deplete the Si layer of free carriers, making the resistivity high. Even for very-high-quality oxide/Si interfaces, the density of these charge traps is of the order of $10^{10}$–$10^{11}\,\mathrm{cm}^{-2}$. In contrast, a 10 nm Si layer that is doped at a typical $10^{15}\,\mathrm{cm}^{-3}$ has only $10^9$ dopant atoms per $\mathrm{cm}^2$. One would therefore predict that measurements depending on the flow of current (such as scanning tunnelling microscopy (STM), electric-force microscopy and Hall effect) and electron emission and reflection processes (such as photoelectron spectroscopy and low-energy electron microscopy) become impossible. Previous reports have, in fact, claimed that surface and interface charge trapping states make STM impossible on thin SOI[8,9]. We show that STM imaging of what is conventionally considered as fully depleted SOI is indeed possible on clean SOI. We demonstrate that electronic conduction is enabled by reconstruction of the clean Si(001) surface, which shifts the Fermi level and results in a population of charge carriers. We suggest that the phenomenon is general if appropriate states are available.

Clean SOI consists of a thin Si layer bounded by two interfaces: Si/$SiO_2$ and Si/vacuum. The Si/$SiO_2$ interface quality is determined by the SOI fabrication process; it is very good indeed in bonded SOI[10]. We used SOI made both by wafer bonding and by the SIMOX process (implant with oxygen and anneal to form a buried oxide). The template layer was doped with boron nominally at $10^{15}\,\mathrm{cm}^{-3}$, and was thinned by dry thermal oxidation at 1,050 °C, followed by wet chemical etching to remove the oxide. To produce thicknesses below 20 nm we used repeated oxidation and oxide etching steps. Very-low-defect-density clean surfaces were produced by removing the final protective oxide via the slow deposition of several monolayers (ML) of Si or Ge at 700 °C in ultrahigh vacuum followed by thermal annealing (see Methods).

Figure 1 shows a schematic diagram of the STM process and images of the surface of several ultrathin-template SOI samples prepared in the above manner. The images shown here were acquired at room temperature in the constant-current mode using a tunnelling current of 0.1 nA. Filled-state and empty-state images of the Si surface were obtained at tip biases of −2 V and +2 V, respectively, relative to the sample. The images are comparable to those obtained from very clean bulk Si(001) at the same bias voltage[11]. The surface reconstructs to form rows of dimerized atoms[12] with alternate orthogonal $(2 \times 1)$ and $(1 \times 2)$ terraces. When we clean the surface with Ge, a zigzag pattern indicative of dimer buckling appears (Fig. 1c) in both filled- and empty-state images, just as in bulk Si(001) on which a small amount of Ge has been deposited[13]. The comparatively rougher Si/$SiO_2$ interface in SIMOX wafers does not affect the quality of STM images of the surfaces of SIMOX template layers (Fig. 1d). Strained SOI also produces outstanding STM images (Fig. 1e).

We wish to use STM as a probe of the conductivity of the thin Si template layer. In order to do so, we must show to what degree this approach is sensible. The two important steps in the conduction of electrons during STM imaging (Fig. 1a) are (1) the tunnelling of an electron from tip to sample (or vice versa) and (2) the subsequent removal of the tunnelling charge to a distant electrical lead to complete the circuit. In the complete absence of the second step, STM is impossible. If a very large sample resistance impedes the second step, imaging will require higher applied voltages. The filled- and empty-state images in Fig. 1 show that on clean SOI STM is not only possible, but requires no excess voltage: the images are acquired with the same minimum voltage used for imaging bulk Si. The effective resistance of the Si layer in STM imaging of thin SOI is thus much less than the tunnelling resistance (20 GΩ) in our STM measurements.

To understand the role a Si/$SiO_2$ interface plays in the Si layer's electronic properties, we analysed the sheet resistance of Si membranes with thicknesses ranging from 15 nm to 200 nm, sandwiched between a native oxide and the buried oxide. The nominal doping level of the Si layer is $10^{15}\,\mathrm{cm}^{-3}$. The interface trap density of states ($D_{\mathrm{it}}$) typically exhibits a 'U' shape across the Si bandgap, with $D_{\mathrm{it}}$ of the order of $10^{10}$ to $10^{11}\,\mathrm{cm}^{-2}\,\mathrm{eV}^{-1}$. Interface traps in the upper half of the bandgap behave as acceptors, while those in the lower half

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behave as donors[14,15]. A thin Si layer is depleted of free carriers, which results in a high sheet resistance. Using the van der Pauw method, we have measured a two-dimensional (2D) resistivity $\rho_{2D} = 80$ GΩ square$^{-1}$ for a 20 nm Si layer sandwiched between a native oxide and the buried oxide, a reasonable value for such thin SOI[16].

The STM imaging occurs, of course, with the top oxide removed. The simplest explanation for the good STM images might be that removal of the top (native) oxide reduces the number of traps by a factor of two, freeing some of the trapped carriers. The Si/$SiO_2$ interface has two orders of magnitude more traps than needed to deplete our samples, however, and therefore a factor-of-two reduction in trap density has an insignificant direct effect on carrier populations. In our STM experiments, the sample electrical lead is far from the tunnelling tip, and the contribution of the sample resistance to the STM circuit is, to a good approximation, the resistance $R$ between two concentric circles, one with the radius at which the current from the tip reaches the sample, $r_1$, and the other at the radius of the contacts, $r_2$, giving:

$$R = \int_{r_1}^{r_2} \rho_{2D} \frac{dr}{2\pi r} = \frac{\rho_{2D}}{2\pi} \ln\left(\frac{r_2}{r_1}\right) \quad (1)$$

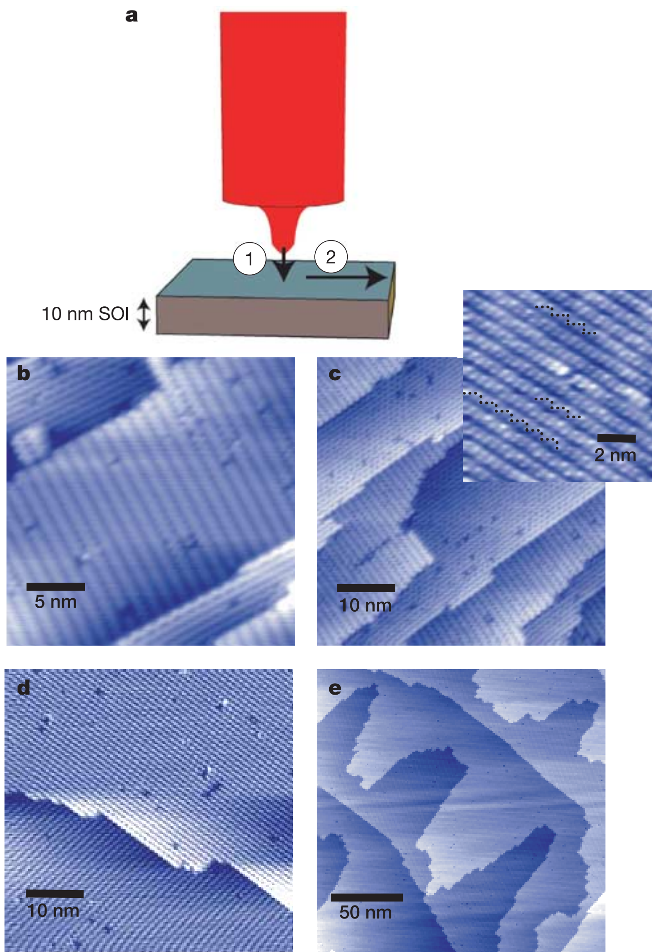


**Figure 1 | Scanning tunnelling microscopy experiment and images of surfaces of clean SOI.** **a**, Schematic diagram of the circuit completed by the tunnelling-gap (1) and sample (2) resistances. **b**, Filled-state STM image of a 10-nm-thick Si template layer in bonded SOI(001) with native oxide removed by ~3 ML of Si (see 'Methods'). **c**, Same as **b** but using Ge to remove the oxide. Inset, empty-state image showing a dimer buckling zigzag pattern produced by a fractional monolayer of Ge remaining in the Si(001) surface. **d**, Filled-state image of the surface of 20-nm-thick SIMOX SOI(001). **e**, Filled-state image of the surface of 15-nm-thick bonded strained SOI(001) (0.8% tensile strain).

The value of $R$ depends only logarithmically on $r_2$ and $r_1$, and therefore details such as the sample shape and the current flow from the tip into the sample are unimportant. Taking reasonable values $r_1 = 1$ nm and $r_2 = 0.5$ cm, we find that $R \approx 2.5\rho_{2D} = 200$ GΩ. This value is far too large, in comparison to the total resistance of the STM circuit, to enable our STM measurements.

An additional conduction mechanism must therefore exist to enable STM on the clean Si(001) template surface. STM imaging is possible because of the influence of the surface π bands formed by the dimer bond reconstruction[17]. Charge transfer inside the tilted dimers on the surface results in an almost filled π band and an almost empty π* band, each with the density of states of about $10^{15}$ cm$^{-2}$ eV$^{-1}$. The gap of about 0.5 eV between these two bands is positioned close to the valence band. This surface gap and the bottom of the π* band pull the Fermi level downward, leading to a large concentration of holes in the Si template layer valence band via thermal excitation of electrons to the π* band. The electronic band structure is shown schematically in Fig. 2 for Si layers with a native oxide and with a clean surface. Conduction in the surface states is immaterial to the Si layer conduction. The conduction of charge carriers by surface states has been probed with a variety of experimental techniques[18–20]. Unless the mobility of electrons in surface bands is large enough to be comparable to the extremely high mobility of holes and electrons in Si, the contribution of surface state conduction to the electronic-transport properties of thin SOI will be negligible.

The combination of the conduction due to holes created in the valence band by excitation of charges into the close-lying empty surface states and the (possibly much lower) conduction of electrons in the surface π* band results in an effective resistance $R_{eff}$ (refs 21, 22):

$$\frac{1}{R_{eff}} = \frac{1}{R'_{bulk}} + \frac{1}{R_{surface}} \quad (2)$$

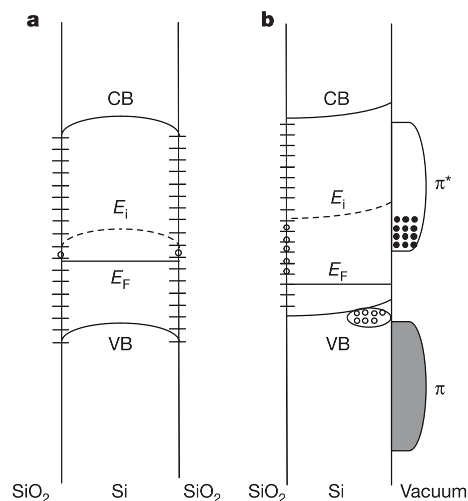


**Figure 2 | Proposed band diagrams showing interface, bulk and surface bands for ultrathin SOI.** **a**, Ultrathin SOI bounded by two Si/$SiO_2$ interfaces. For a 10 nm Si film, the maximum band bending is <100 μeV (grossly exaggerated in the figure). The Fermi level is ~25 meV below the intrinsic level. **b**, Ultrathin SOI bounded by the reconstructed Si(001) surface on one face. The existence of the surface bands results in a dramatically reduced effective bandgap (~0.3 eV) between the (bulk) valence band of the thin Si layer and the surface π* band. The enhanced conductivity is derived from the corresponding thermal population of carriers in those two bands. For a 10 nm Si film, the maximum band bending is ~7 meV. The Fermi level is ~0.4 eV below the intrinsic level at the Si/$SiO_2$ interface. CB, conduction band; VB, valence band; $E_F$, Fermi energy (Fermi level); $E_i$, energy of centre of bandgap (intrinsic level). Short lines denote interface trap states. Holes are indicated by open circles, and in **b** electrons are indicated by filled circles.



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where $1/R'_{bulk}$ is the conductance arising from the thermal population of holes created by repositioning the Fermi level, and $1/R_{surface}$ is the conductance arising from the thermal population of electrons in the surface $\pi^*$ states. Carriers at the buried $Si/SiO_2$ interface are effectively immobile.

The value of $R_{eff}$ is much less than the 200 GΩ found for oxidized surfaces. For the range of acceptable values of the density of interface traps, $D_{it}$, from Fermi distribution calculations, the hole concentration in the valence band of the 10 nm SOI layer is $(2–4) \times 10^{10}\,cm^{-2}$, the electron density in the $\pi^*$ band is $(4.4–6) \times 10^{10}\,cm^{-2}$, and the net remaining charge is in the form of trapped holes at the $Si/SiO_2$ interface. The overall distribution of charges is summarized in Fig. 2b. Charge carriers in the Si valence band and at the surface are able to respond to applied electric fields, and the calculated carrier concentrations are a basis for a quantitative comparison of $R'_{bulk}$ and $R_{surface}$. The high-mobility holes are not influenced by the orientation of the local surface reconstruction.

Figure 3 shows the variation of the sheet resistance as a function of Si(001) template layer thickness in SOI. The top curve is a fit to the measured resistivity of the Si(001) layer bounded by oxide on both sides. The bottom curve is a calculation of the sheet resistance for a Si(001) layer with a clean reconstructed surface. The predictions of Fig. 3 are based on a numerical estimate of the band bending, assuming a surface density of states given by first-principles calculations of the Si(001) surface electronic structure[17]. We have assumed a density of states at the $Si/SiO_2$ interface that is consistent with previous measurements[10]. When the high mobility of carriers introduced into the Si 'bulk' by the surface bands is considered, the resistivity is considerably lower than the expected resistivity due to dopants alone for all Si film thicknesses below 70 nm. For both the oxide- and the vacuum-terminated ultrathin SOI, the bulk doping density is virtually irrelevant for electronic properties.

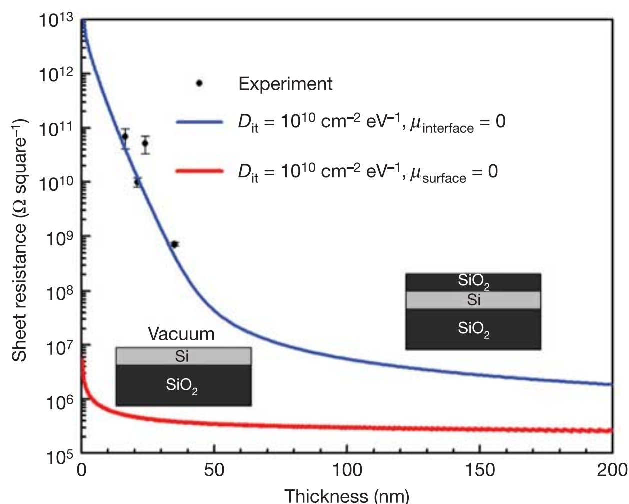


**Figure 3 | Sheet resistance, as function of the Si layer thickness, of a thin Si membrane with different bounding layers.** Upper curve, bounded by two $Si/SiO_2$ interfaces (right inset structure diagram); lower curve, bounded on one side by a clean reconstructed Si(001) surface (left inset structure diagram). Error bars (±s.d.) give the uncertainty in the measured sheet resistance values—they are higher for higher resistances. The upper curve is a fit to the resistance measurements, requiring a density of local interface trap states $D_{it} = 1.1 \times 10^{10}\,cm^{-2}\,eV^{-1}$, a value that corresponds to high-quality $Si/SiO_2$ interfaces and an interface state mobility, $\mu_{interface}$, of zero. The lower curve is calculated with the same $D_{it}$ and assuming that the mobility of carriers in the surface states, $\mu_{surface}$, is negligible. The sheet resistance is not sensitive to the value of the surface state mobility: even a very high surface state mobility has an insignificant effect on the total conductivity. For very thin Si membranes, therefore, the existence of appropriate surface bands leads to a conductivity dramatically higher than expected for a thin layer of Si with two oxide terminations. A difference in sheet resistance of at least an order of magnitude persists to large Si membrane thicknesses.

It is thus the interaction between surface and bulk that enables high-mobility conduction in nanoscale SOI. This interaction suggests that conduction in even the thinnest membranes or layers of Si(001) is possible, independent of any considerations of bulk band structure, defect states, and doping, as long as at least one Si membrane or layer surface or interface produces states that move the Fermi level sufficiently to enable the thermal excitation of 'bulk' carriers in the Si. In the present case that is a surface clean enough to produce the dimer reconstruction and surface electronic bands, but many other possibilities suggest themselves. For example, organic thin films can be tailored to have bandgaps with a lowest unoccupied molecular orbital or conduction band close to the Si valence band. The Si membrane layer will become hole doped, exactly as we describe here for a clean surface. The conduction properties of the organic layer (or whatever interface layer is created) are irrelevant. In addition to organic–inorganic interfaces, epitaxial insulators or insulators that form a disordered interface with Si provide practical examples of situations in which bulk conduction may be enabled by states at a surface or interface.

Conduction will be possible in very thin layers or membranes of other materials when the surface Fermi level is pinned far from mid-bandgap by surface or interface states. Considerations of the density of bulk dopants become irrelevant as long as the doping is not degenerate. For materials that have inappropriate surface states, such as cleaved GaAs(110), measurements that depend on electron transport may fail in thin enough films or membranes if interface trap states deplete the bulk carriers. If a material is deposited that provides these states, the conduction becomes enabled.

As we have described, in our clean-Si layers, conduction through the Si layer is enabled by interaction with the surface states created by reconstruction, as demonstrated with STM measurements. STM imaging will be possible on SOI(001) at any Si layer thickness at which the surface bands are well developed. In our situation, disruption of the surface bands will prevent STM imaging (or other forms of imaging requiring electron transport) of the thin SOI(001). Disruption of the $\pi$-bonded dimer chains that produce the surface bands can come, for example, via introduction of surface structural disorder, chemisorption of H (ref. 23) and other gases[24], or oxidation[22,25]. Previous efforts to image SOI(001) with STM have encountered contamination and apparent disruption of these surface states, removing the surface state–bulk interaction that enables high-mobility conduction[8,9]. The surface state–bulk interaction could be preserved outside vacuum using approaches that leave the surface chemically protected, but preserve the dimer structural motif and the high density of surface states[26,27].

In materials with appropriate surface or interface bands to allow thermal interaction with bulk bands, arbitrarily thin membranes or layers should show electronic conduction. Electronic-transport measurements (including, but not limited to, STM) should permit study of the transition from thin but still conventional layer structures to potentially novel phases created by the interaction of front and back layer interfaces.

## METHODS

Surface preparation of ultrathin SOI for STM imaging consists of *ex situ* and *in situ* cleaning. *Ex situ*, the SOI is triple IMEC cleaned[28]. A final 'Piranha' (mixture of $H_2SO_4$ and $H_2O_2$, 2–4:1) clean is performed to terminate the surface with a thin (1–2 nm) oxide for protection as the sample is transported to the chamber. The samples are introduced into an ultrahigh-vacuum STM, with a base pressure below $1 \times 10^{-10}$ torr. Traditional *in situ* preparation of surfaces by direct heating to 1,500 K for several minutes used for bulk Si is not possible for SOI because the Si template layer dewets. Instead, we slowly deposit several ML of Si or Ge at 700 °C at 0.5 ML min$^{-1}$ to remove the oxide. Finally we flash the sample to 800 °C (below the critical temperature for Si film dewetting) for two minutes, quench and anneal it at 600 °C for 30 min, radiation cool it, and transfer it to our STM chamber.


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1. Lu, Z. H., Lockwood, D. J. & Baribeau, J. M. Quantum confinement and light-emission in $SiO_2$/Si superlattices. *Nature* **378,** 258–260 (1995).
2. Legrand, B., Agache, V., Nys, J. P., Senez, V. & Stievenard, D. Formation of silicon islands on a silicon on insulator substrate upon thermal annealing. *Appl. Phys. Lett.* **76,** 3271–3273 (2000).
3. Liu, W. & Asheghi, M. Phonon-boundary scattering in ultrathin single-crystal silicon layers. *Appl. Phys. Lett.* **84,** 3819–3821 (2004).
4. Liu, F., Huang, M. H., Rugheimer, P. P., Savage, D. E. & Lagally, M. G. Nanostressors and the nanomechanical response of a thin silicon film on an insulator. *Phys. Rev. Lett.* **89,** 136101 (2002).
5. Celler, G. K. & Cristoloveanu, S. Frontiers of silicon-on-insulator. *J. Appl. Phys.* **93,** 4955–4978 (2003).
6. Kim, Y. A 0.25 mm 600MHz 1.5V SOI 64b ALPHATM microprocessor. *ISSCC Dig. Tech. Pap.* **I,** 432–433 (1999).
7. Yan, R. H., Ourmazd, A. & Lee, K. F. Scaling the Si MOSFET — From bulk to SOI to bulk. *IEEE. Trans. Electron. Dev.* **39,** 1704–1710 (1992).
8. Sutter, P., Ernst, W. & Sutter, E. Scanning tunneling microscopy on ultrathin silicon on insulator (100). *Appl. Phys. Lett.* **85,** 3148–3150 (2004).
9. Lin, K. C., Holland, O. W., Feldman, L. C. & Weitering, H. H. Surface characterization of silicon on insulator material. *Appl. Phys. Lett.* **72,** 2313–2315 (1998).
10. Hovel, H. *et al.* Status of 300 mm SOI material: comparisons with 200 mm. *Proc. Electrochem. Soc.* **2003–05,** 75–80 (2003).
11. Swartzentruber, B. S., Kitamura, N., Lagally, M. G. & Webb, M. B. Behavior of steps on Si(001) as a function of vicinality. *Phys. Rev. B* **47,** 13432–13441 (1993).
12. Tromp, R. M., Hamers, R. J. & Demuth, J. E. Si(001) dimer structure observed with scanning tunneling microscopy. *Phys. Rev. Lett.* **55,** 1303–1306 (1985).
13. Fontes, E., Patel, J. R. & Comin, F. Direct measurement of the asymmetric dimer buckling of Ge on Si(001). *Phys. Rev. Lett.* **70,** 2790–2793 (1993).
14. Schroder, D. K. *Semiconductor Material and Device Characterization* (Wiley & Sons, New York, 1998).
15. McWhorter, P. J. & Winokur, P. S. Simple technique for separating the effects of interface traps and trapped-oxide charge in metal-oxide-semiconductor transistors. *Appl. Phys. Lett.* **48,** 133–135 (1986).
16. Cristoloveanu, S. & Sheng, L. *Electrical Characterization of Silicon-on-Insulator Materials and Devices* (Kluwer, Boston, 1995).
17. Northrup, J. E. Electronic structure of Si(100)C(4x2) calculated within the GW approximation. *Phys. Rev. B* **47,** 10032–10035 (1993).
18. Stroscio, J. A. & Ho, W. Long-range quasielastic scattering of low-energy electrons by conduction-band surface-plasmons on Si(111)7x7. *Phys. Rev. Lett.* **54,** 1573–1576 (1985).
19. Heike, S., Watanabe, S., Wada, Y. & Hashizume, T. Electron conduction through surface states of the Si(111)-(7x7) surface. *Phys. Rev. Lett.* **81,** 890–893 (1998).
20. Tanikawa, T., Matsuda, I., Kanagawa, T. & Hasegawa, S. Surface-state electrical conductivity at a metal-insulator transition on silicon. *Phys. Rev. Lett.* **93,** 016801 (2004).
21. Petersen, C. L., Grey, F., Shiraki, I. & Hasegawa, S. Micro-four-point probe for studying electronic transport through surface states. *Appl. Phys. Lett.* **77,** 3782–3784 (2000).
22. Yoo, K. & Weitering, H. H. Electrical conductance of reconstructed silicon surfaces. *Phys. Rev. B* **65,** 115424 (2002).
23. Chen, D. X. & Boland, J. J. Chemisorption-induced disruption of surface electronic structure: Hydrogen adsorption on the Si(100)-2x1 surface. *Phys. Rev. B* **65,** 165336 (2002).
24. Chen, D. X. & Boland, J. J. Spontaneous roughening of low-coverage Si(100)-2x1: Cl surfaces: Patch formation on submonolayer halogenated surface. *Phys. Rev. B* **70,** 205432 (2004).
25. Hollinger, G. & Himpsel, F. J. Oxygen chemisorption and oxide formation on Si(111) and Si(100) surfaces. *J. Vac. Sci. Technol. A* **1,** 640–645 (1983).
26. Hamers, R. J. *et al.* Cycloaddition chemistry of organic molecules with semiconductor surfaces. *Acc. Chem. Res.* **33,** 617–624 (2000).
27. Seino, K., Schmidt, W. G. & Bechstedt, F. Organic modification of surface electronic properties: A first-principles study of uracil on Si(001). *Phys. Rev. B* **69,** 245309 (2004).
28. Meuris, M. *et al.* The IMEC clean — A new concept for particle and metal removal on Si surfaces. *Solid State Technol.* **38,** 109–114 (1995).

**Supplementary Information** is linked to the online version of the paper at www.nature.com/nature.

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