Enhanced hole mobility in ambipolar rubrene thin film transistors on polystyrene

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We report amorphous rubrene thin film transistors with a polystyrene intermediate layer on the SiO_2 gate dielectric that have hole mobilities up to 0.01 $cm^2/V\,s$. This improvement by two orders of magnitude over devices formed on SiO_2 alone occurs without the crystallization of rubrene. The enhanced charge transport is a result of the more planar growth and subsequent better geometrical connection of the first molecular layers of rubrene. Ambipolar conduction in the rubrene suggests that polystyrene minimizes the concentration of interfacial electron trap states. © *2008 American Institute of Physics*. [DOI: 10.1063/1.2904964]

Rubrene thin film transistors offer the potential to adapt the high mobility of rubrene single crystal field effect devices to thin film electronics.[1] So far, although the field effect mobility in rubrene single crystal transistors can be up to 15 $cm^2/V\,s$, the corresponding mobility in amorphous rubrene thin films on SiO_2 is four to five orders of magnitude lower.[2,3] An important strategy to address this difference has been to create crystalline rather than amorphous thin films. Rubrene thin films can be crystallized at elevated temperatures, or by depositing films onto heated substrates or buffer layers.[4,5] The mobility of holes in these devices is higher than in devices with amorphous rubrene thin films, reaching nearly 1 $cm^2/V\,s$.[4,6] In this letter, we show that the growth process can be further manipulated using ideas derived from the surfactant effect originally discovered in inorganic epitaxial growth,[7] and that a change in the morphology alone can have important electrical consequences.

In addition to the lack of crystallinity, the morphology of amorphous rubrene thin films is quite different from other organic semiconductors. Pentacene, in particular, forms a two-dimensional layer one molecule thick on SiO_2 with a hole mobility nearly as high as thicker films.[8] Rubrene does not form a low-energy interface with SiO_2 and as a result forms large spherical islands immediately.[2] Here, we show that the morphology of an amorphous rubrene film can be manipulated using a polystyrene (PS) layer between the rubrene and SiO_2 and that the improved morphology dramatically changes the transport characteristics of a rubrene thin film devices. The rubrene field effect transistors (FETs) were fabricated on a 200 nm thick SiO_2 gate dielectric on a highly *p*-type silicon substrate which functioned as the gate electrode. Source and drain electrodes were fabricated using photolithography using 60 nm thick Au films on a 1 nm thick Cr adhesion layer. The channels of the FET devices were 800 μm wide and from 100 to 300 μm long.

Rubrene is a nonpolar organic compound and can be expected to form low-energy interfaces with other nonpolar materials, including PS. Prior to the deposition of rubrene, our bottom-contact FET devices were coated with a 30 nm PS layer by spin coating from a 1 wt % solution of PS in toluene, at 4000 rpm and a deposition time of 1 min. PS is an ideal interfacial layer because PS can be deposited on SiO_2 with a low root-mean-square (rms) roughness.[9] Pentacene transistors on PS can have a higher mobility than on smooth SiO_2.[9] The surface of the PS layer exhibited a number of randomly distributed pits, as in the atomic force microscopy (AFM) image in Fig. 1(a). The rms roughness in the regions away from the pits was 0.3 nm. Similar pits have been attributed to poor wetting of thin polymer films on SiO_2 and to the presence of isolated impurities on the surface.[10] The contact angle for water on the PS surface was 97.6°, which is consistent with values previously reported for spin-coated PS films.[11] Rubrene thin films were deposited at a rate of 1 nm/min using thermal evaporation in a vacuum chamber with a base pressure of 6×10^{-7} torr. All electrical measurements were performed in vacuum at room temperature.

Rubrene thin films on the PS layer have a different morphology than films on SiO_2. On SiO_2, rubrene forms islands that are isolated from each other by large areas of exposed SiO_2 [Fig. 1(b)]. The islands can reach heights of tens of nanometers before coming into contact. On PS, rubrene

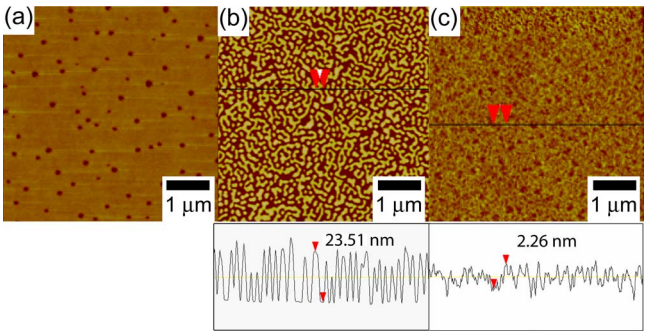

FIG. 1. (Color online) AFM image of (a) a PS film on SiO_2, and rubrene thin films on (b) SiO_2 and (c) PS. The difference in rubrene morphology between films on SiO_2 and PS is visible in the cross sections plotted below (b) and (c).

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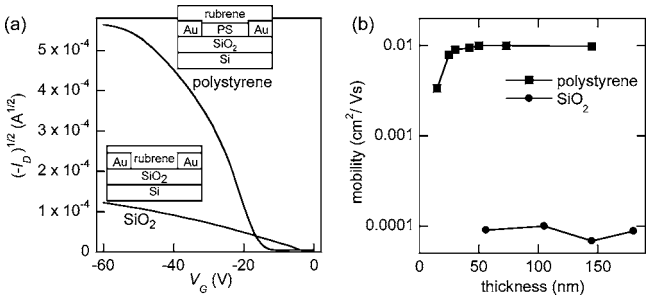

FIG. 2. (a) Transistor characteristics of 145 nm thick rubrene films deposited on SiO_2 (circles) and PS (squares). (b) The mobility of holes in the saturation regime of transistor operation as a function of the average thickness of the rubrene film. The channel length for this device was 100 μm.

forms smaller islands that complete a connected film at a much smaller average thickness [Fig. 1(c)]. The rms roughness of rubrene on PS is 1 nm, which is consistent with the formation of a continuous film. The role of the PS layer is analogous to the role of atomic surfactants in molecular beam epitaxy, in which changes in the surface energy can change the thermodynamically favored morphology of a subsequent thin film.[7]

Figure 2 compares the electrical characteristics of a rubrene transistor on SiO_2 with a transistor formed on PS. The field effect mobility was measured from these current-voltage characteristics in the saturation regime using a linear fit to a plot of the square root of the drain current I_D as a function of the gate voltage V_G.[12] The mobility of holes in the rubrene film on SiO_2 was 6.8×10^{-5} cm^2/V s, which is much lower than rubrene single crystal transistors, but comparable to previous rubrene FETs on SiO_2.[2] The mobility of holes in the rubrene film on PS was 9.9×10^{-3} cm^2/V s, more than two orders of magnitude larger than for rubrene on SiO_2. The improvement in mobility occurred without the crystallization of the rubrene layer. We did not observe any optical or AFM signature of crystallization as reported by Hsu *et al.*[4] or Seo *et al.*[6] Surface x-ray diffraction studies at the Advanced Photon Source of Argonne National Laboratory showed no signs of crystalline x-ray reflections.

A second effect of the change in the morphology induced by PS is in the evolution of the electrical properties as a function of the total amount of rubrene deposited on the surface. In Fig. 2(b), the mobility of holes is plotted as a function of the average thickness of rubrene on SiO_2 and PS. The average thickness given in Fig. 2(b) is the product of the rubrene deposition rate, measured in an AFM image at low rubrene coverage, and the deposition time. The mobilities were measured for one FET on each substrate during pauses in the deposition of rubrene. After the initial geometric percolation of rubrene islands at 50 nm on SiO_2 and 10 nm on PS, the hole mobility was independent of the rubrene thickness. At all thicknesses, the mobility of holes in rubrene films on SiO_2 and PS differ by two orders of magnitude. The higher layers of rubrene on the SiO_2 surface, which has a poor initial connection between rubrene islands, do not improve the crucial first few molecular layers.

Rubrene transistors on PS exhibit ambipolar transport. Figure 3 shows transfer characteristic curves of rubrene ambipolar FETs at drain voltages of −60 and 60 V for *p*-channel and *n*-channel operations, respectively. In Fig. 3(a), the hole current observed at high negative gate voltages increased with further increases in the magnitude of the gate

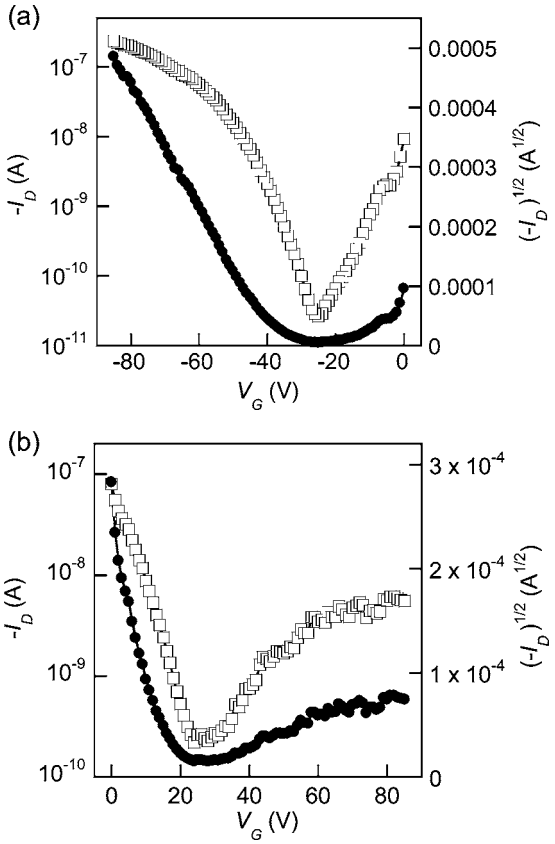

FIG. 3. Plots of $-I_D$ vs V_G (squares) and $(-I_D)^{1/2}$ vs V_G (circles) for (a) *p*- and (b) *n*-channel operations. The drain voltages for (a) and (b) are −60 and 60 V, respectively. The channel length for this device was 300 μm.

voltage. An electron current was observed with positive polarity, which is typical of ambipolar FETs.[13,14] The threshold voltage for holes from the linear fit of V_G as a function of $-I_D^{1/2}$ in the saturation regime is −38 V. The onset of electron current occurred at a gate voltage V_G of −25 V. Figure 3(b) shows *n*-type operation in the saturation regime, where there is an electron current for positive gate voltages and a hole current for negative gate voltages. The threshold voltage for electron transport was 19 V. The hole and electron mobilities for this device were 4.7×10^{-3} and 7.9×10^{-5} cm^2/V s, respectively.

The efficient transfer of electrons from contacts into organic materials is far more difficult than the transfer of holes because of the mismatch between the work functions of common metals and the relevant energy levels of organic semiconductors. This effect can lead to lower effective mobilities in devices, independent of the efficiency with which electrons are transported through the organic semiconductor. In our previous work with rubrene on SiO_2, we found that the lower work function of Cr resulted in a lower barrier for the injection of electrons into rubrene films.[3] Similarly, *n*-channel operation can be observed in rubrene single crystals and pentacene thin films with Ca contacts.[13,15]

In addition, electrons are far more easily trapped than holes at chemical defects in the semiconductor and in states at dielectric interfaces, such as hydroxyl groups on the surface of SiO_2 gate dielectrics.[16] Estimates in the literature of SiOH concentration ($\sim4\times10^{13}$ cm^{-2}) on SiO_2 surfaces, for example, are comparable to the charge density (10^{13} cm^{-2}) in a FET operating at V_G=100 V, and could lead to threshold voltages of approximately that magnitude.[17] Trapped elec-

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trons effectively compensate the gate voltage applied and prevent the observation of electron transporting behavior by shifting the threshold voltage for *n*-channel operation to unattainable values. As a result, unless the electron affinity of organic active layers is higher than 3.85 eV, only hole carriers can be readily observed with gate dielectrics on which there is a high concentration of hydroxyl groups.[16]

Because the 1 nm Cr adhesion layer of the source and drain contacts in the device formed on PS is likely covered by the 30 nm PS layer, we infer that electrons were injected from Au to rubrene layers. In this case, despite the relatively high barrier for electron injection from Au, we hypothesize that the electron current was observable due to the low density of electron traps on PS and that the low electron mobility in the rubrene FETs on PS is due to the poor electron injection from Au electrodes. The electron mobilities in these devices are comparable to those on SiO_2 even though the morphology of rubrene is more favorable to charge transport. The threshold voltage for electron current on PS devices, 19 V, is small, however, compared to values near 100 V obtained in rubrene FETs on SiO_2 without PS.[3]

The ambipolar behavior of rubrene on both SiO_2 and PS disappeared after the devices were exposed to air. A similar effect is observed in FETs based on C_{60}, also an electron transporting material, and attributed to contamination of the C_{60} film.[18] In pentacene thin films, *n*-channel behavior has been linked to the chemical purity of the pentacene starting material.[13] Similarly, for rubrene, the disappearance of the *n*-channel behavior may be similarly due to the accumulation of impurities at the PS/rubrene interface or in the rubrene thin film when the device is exposed to air.

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[1] V. C. Sundar, J. Zaumseil, V. Podzorov, E. Menard, R. L. Willett, T. Someya, M. E. Gershenson, and J. A. Rogers, Science **303**, 1644 (2004).
[2] V. Podzorov, V. M. Pudalov, and M. E. Gershenson, Appl. Phys. Lett. **82**, 1739 (2003).
[3] S. Seo, B.-N. Park, and P. G. Evans, Appl. Phys. Lett. **88**, 232114 (2006).
[4] C. H. Hsu, J. Deng, C. R. Staddon, and P. H. Beton, Appl. Phys. Lett. **91**, 193505 (2007).
[5] S.-W. Park, S. H. Jeong, J.-M. Choi, J. M. Hwang, J. H. Kim, and S. Im, Appl. Phys. Lett. **91**, 033506 (2007).
[6] J. H. Seo, D. S. Park, S. W. Cho, C. Y. Kim, W. C. Jang, C. N. Whang, K.-H. Yoo, G. S. Chang, T. Pedersen, A. Moewes, K. H. Chae, and S. J. Cho, Appl. Phys. Lett. **89**, 163505 (2006).
[7] M. Copel, M. C. Reuter, E. Kaxiras, and R. M. Tromp, Phys. Rev. Lett. **63**, 632 (1989).
[8] B.-N. Park, S. Seo, and P. G. Evans, J. Phys. D **40**, 3506 (2007).
[9] S. E. Fritz, T. W. Kelley, and C. D. Frisbie, J. Phys. Chem. B **109**, 10574 (2005).
[10] G. Reiter, Phys. Rev. Lett. **68**, 75 (1992).
[11] S. Wu, *Polymer Interface and Adhesion* (Dekker, New York, 1982).
[12] S. M. Sze, *Physics of Semiconductor Devices* (Wiley, New York, 1981).
[13] C. Rost, D. J. Gundlach, S. Karg, and W. Rieb, J. Appl. Phys. **95**, 5782 (2004).
[14] T. Yasuda, T. Goto, K. Fujita, and T. Tsutsui, Appl. Phys. Lett. **85**, 2098 (2004).
[15] T. Takenobu, T. Takahashi, J. Takeya, and Y. Iwasa, Appl. Phys. Lett. **90**, 013507 (2007).
[16] L. L. Chua, J. Zaumseil, J. F. Chang, E. C.-W. Ou, P. K.-H. Ho, H. Sirringhaus, and R. H. Friend, Nature (London) **434**, 194 (2005).
[17] Y. Nagasawa, I. Yoshii, K. Naruke, K. Yamamoto, H. Ishida, and A. Ishitani, J. Appl. Phys. **68**, 1429 (1990).
[18] R. C. Haddon, A. S. Perel, R. C. Morris, T. T. M. Palstra, A. F. Hebard, and R. M. Fleming, Appl. Phys. Lett. **67**, 121 (1995).

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